

Title	Page
Cover Sheet	1
Block Diagram/Device Map/GPIO Table/Clock Distribution	2-5
CPU-CLK/Control/MISC/PEG/CPU-Memory	6-7
CPU-Power/CPU-GND	8-9
DDR III DIMM 1 / 2,DDR III DIMM 3 / 4	10-11
CLK GEN4116	12
PCH-PCI/E/DMI/USB/CLK	13
PCH-SATA/HOST/FAN/GPIO/VGA	14
PCH-SMB/LPC/AUDIO/RTC/RST	15
PCH-POWER,GND/NVRAM	16-17
SIO-Fintek F71889F/KB/FDD	18
PLX8608	19
PCIE x16 & x1 Slots	20
PCIEx8/Pericom switch	21
PCI Slot 1 & 2	22
1394 Controller - VT6315N-CE	23
JMB-363 SATA X2/ IDE X1	24
LAN-RTL8111DL_1	25
LAN-RTL8111DL_2	26
MARVELL SATA 6G	27
NEC USB3.0	28
Audio Codec ALC889	29
SATA / FAN Control	30
USB Connector	31
ATX F_Panel/EMI/TPM	32
ACPI Controller UPI	33
CPU_VTT - uP6212 2-Phase	34
DDR Power - uP6103 1-Phase	35
PCH & 8608 Power - uP6103	36
VRD11.1 - UP6208 8-Phase,(Dr.Mos)	37-38
Power Meter/CPU LED	39
NCT3016Y	40
CPU XDP & TOUCH PAD	41
Manual & Option	42
Manual & Option	42
Manual & Option	42
Manual & Option	42
Manual & Option	42

MS-7585

ATX

Ver: 1.1

CPU:
INTEL -HAVENDALE/Lynnfied LGA 1156

System Chipset:
INTEL-IBEXPEAK PCH

OnBoard Chipset:
Clock Gen:IDT 4116
HD Audio Codec:RTL889
LAN:RTL 8111DL 10/100/1000 NIC X 2
SIO:FIN71889
Flash ROM: 32 Mb SPI (CHIP)

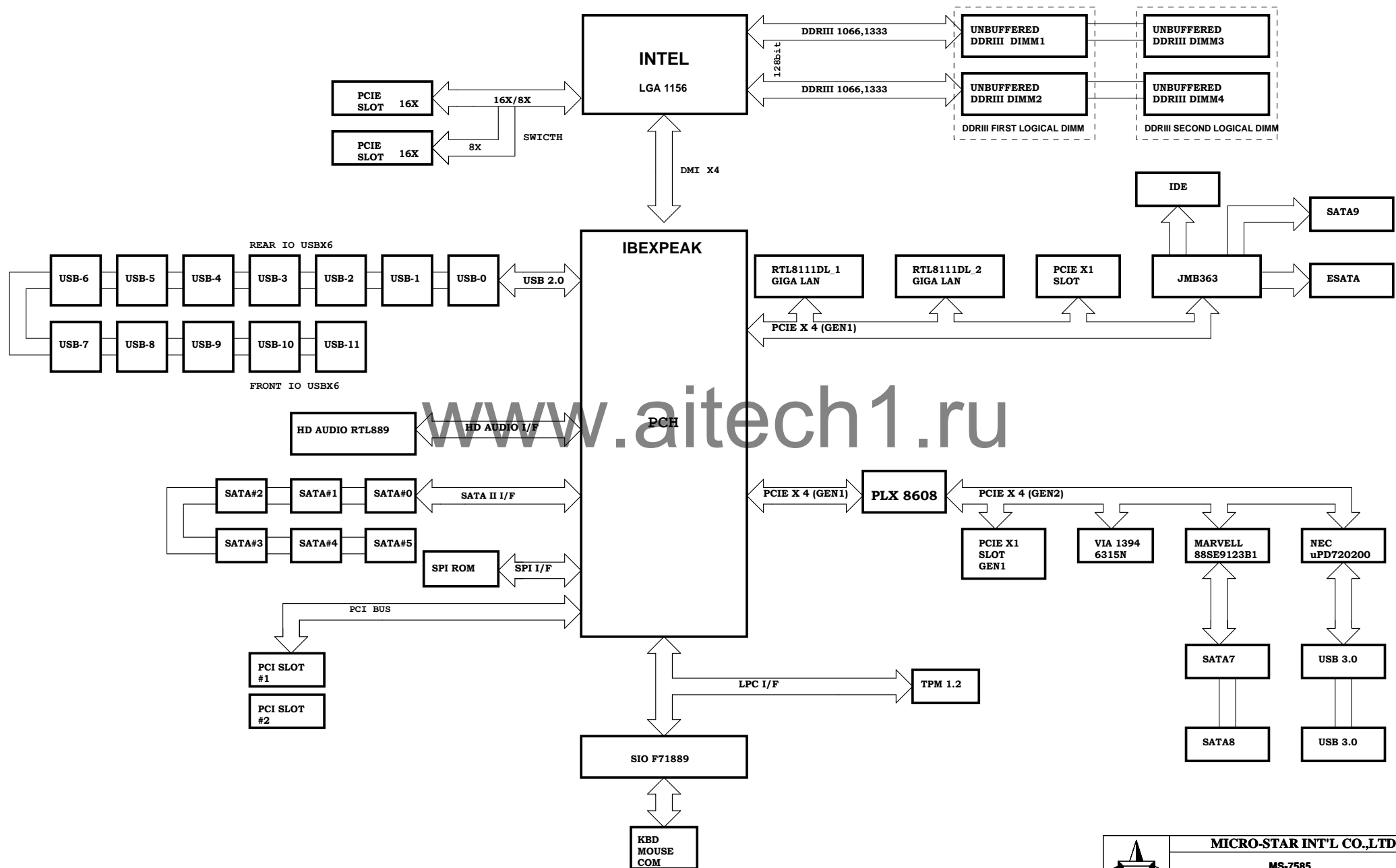
Main Memory:
DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:
PCI Express (X16) Slot * 1
PCI Express (X8) Slot * 1
PCI Express (X1) Slot * 2
PCI Slot * 2

PWM:
Controller:uP6218 (8-Phase 95W)
Controller:uP6212

ACPI:
UPI

Other:
SATA(SATA2-300MB/s) *6
SATA(JMB363 SATA2-300MB/s) *2
USB2.0 *12 (Rear*6 Front*6)
COM Header *1
NEC uPD720200 USB3.0 *
MARVELL SATA 6G*2
1394 Controller - VT6315N-CE



DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 4 CH-A	10100010B	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2
DIMM 3 CH-B	10100011B	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#E PCI_INT#F PCI_INT#G PCI_INT#H	PCI_REQ0# PCI_GNT0#	AD16	CLK33M_PCISLOT_J20
TPM				LPCCLK0
SIO				LPCCLK1

TABLE 9-4
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #3	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

PCI RESET DEVICE

IBEXPEAK	
Signals	Target
PCIRST#	PCISLOT1
PE_RST#	TPM_RST#
PE_RST#	LPC/SIO

www.aitech1.ru

Pin		GPIO	POWER WELL	IO	Function	Implementation	Function
AK41	GPIO0	MAIN	I	BMBSY#	Pull-up to +3.3V and connect to the PECT1 REQ# pin (TBD) on the SIO	PECT1 REQ#	
AL14	GPIO1	MAIN	I	TACH1	Through a 0Ω series resistor, connect to one of the front fan's TACH interface circuit.	TACH1	
AW8	GPIO2	MAIN	I	PCL1REQ#	See PCA Spec	PCI Interrupt E#	
AW7	GPIO3	MAIN	I	PCL1REQ#	See PCA Spec	PCI Interrupt F#	
AP12	GPIO4	MAIN	I	PCL1REQ#	See PCA Spec	PCI Interrupt G#	
AW4	GPIO5	MAIN	I	PCL1REQ#	See PCA Spec	PCI Interrupt H#	
AY11	GPIO6	MAIN	I	TACH2	Pull-up to +3.3V and connect to P52 pin 12. The COMM B assembly connects pin 12 directly to GND	COMM_B_DET#	
AY11	GPIO7	MAIN	I	TACH3	Through a 0Ω series resistor, connect to one of the front fan's TACH interface circuit.	TACH3	
AK30	GPIO8	RESUME	O	IOCS_EN#		Reserved	
AL28	GPIO9	RESUME	I	OC5	Associated with USB port 05 powerwell. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#	
AL30	GPIO10	RESUME	I	OC6	Pull-up to +3.3VSB and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID2	
AL31	GPIO11	RESUME	I	SMBALERT#	Pull-up to +3.3VSB. It is always enabled as a wake event.	SMBALERT#	
AW34	GPIO12	RESUME	I	LAN_DISABLE	Follow implementation in Intel Pitkin Design Guide	LAN_DISABLE#	
AR16	GPIO13	RESUME	I	IO_PME	Pull-up to +3.3V SB and connect to P151-pin 10; also add a no-installed pulldown to the net.	RDYBST_DET# or DASH SMI	
AM30	GPIO14	RESUME	I	OC7	Pull-up to +3.3VSB and connect to the SMI pin on the SIO	SMI# from SIO	
AY36	GPIO15	RESUME	I	PCH_GPI5		Reserved	
AW39	GPIO16	RESUME	O	SATAACP	Follow implementation in Intel Pitkin Design Guide	CPU_MISSING	
AW11	GPIO17	MAIN	I	TACH0	Through a 0Ω series resistor, connect to one of the front fan's TACH interface circuit.	TACH0	
AW39	GPIO18	MAIN	I	PCL1KRQ1#	Through a 1KΩ series resistor, pull-up to +3.3V and connect to E15-pin 1.	BOOT_BLK_REC#	
AW38	GPIO19	MAIN	I	SATA1CP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID1	
AP18	GPIO20	MAIN	I	PCL1KRQ2#		PCIECLKRQ2#	
AT37	GPIO21	MAIN	I	SATA0GP	Pull-up to +3.3V and connect to P23-pin 4.	FRNT_AUD_DET#	
AN41	GPIO22	MAIN	I	SCLOCK	Pull-up to +3.3V and connect to P150-pin 10	INT_USB_DET#	
AP14	GPIO23	MAIN	I	LDRQ1#	Pull-up to +3.3V and connect to the PCI SLOT Riser Detect circuit.	RISER_DET#	
AR34	GPIO24	RESUME	O	MEMLED	Through a 1KΩ series resistor, pull-up to +3.3VSB and connect to P125-Pin 1	HOOD_SW_DET#	
AP33	GPIO25	RESUME	I	PCL1KRQ3#		PCIECLKRQ3#	
AW37	GPIO26	RESUME	I	PCL1KRQ4#		PCIECLKRQ4#	
AP37	GPIO27	RESUME	O	OD_PLL_VR_EN		Reserved	
AY40	GPIO28	RESUME	O	PCH_GPI2			
BA35	GPIO29	RESUME	O	SLP_LAN#	Connect to a circuit used to force the 3.3V_CL rail on.	WOL_EN	
AT37	GPIO30	RESUME	I	SUS_PWR_ACK			
AW40	GPIO31	MAIN	I	ACPRESENT	TBD. For now connect to a Test Point	ESATA_DET#	
AW40	GPIO32	MAIN	O	PCH_GPI2	Through a 1KΩ series resistor, pull-up to +3.3V and connect to P1-pin 20.	SSX_PS_DET#	
AT16	GPIO33	MAIN	O	PCH_GPI3	Through a 1KΩ series resistor, pull-up to +3.3V and connect to pin 1 of Jumper E1	FDT_BVRD#	
AT40	GPIO34	MAIN	O	SP_PCV	Pull-down to GND and connect to P124-pin 2. Decouple with 0.1μF	HOOD_LOCK_DET	
AW41	GPIO35	MAIN	O	SATA1KREQ#	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV0	
AW39	GPIO36	MAIN	I	SATA2CP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_REV1	
AW38	GPIO37	MAIN	I	SATA3GP	Pull-up to +3.3V and connect to P126-pin 16	PRNTR_DET#	
AW38	GPIO38	MAIN	I	SLOAD	Through a series 1K resistor, connect to P5-pin 9 and pull-up to +3.3V	CHASSIS_ID0	
AT39	GPIO39	MAIN	I	SDATAOUT0	Pull-up to +3.3V and connect to top-layer ring of PCA mounting hole used for SFF Basepan detect feature.	BASEPAN_DET#	
AT30	GPIO40	RESUME	I	OC1	Using an 8.2KΩ resistor, pull-down to GND and connect to E49-pin 2	PASSWORD_EN	
AK28	GPIO41	RESUME	I	OC2	Associated with USB port 2 powerwell. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#	
AP30	GPIO42	RESUME	I	OC3	Associated with USB port 3 powerwell. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#	
AP31	GPIO43	RESUME	I	OC4	Associated with USB port 4 powerwell. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#	
AW38	GPIO44	RESUME	I	PCL1KRQ5#		PCIECLKRQ5#	
AW36	GPIO45	RESUME	I	PCL1KRQ6#		PCIECLKRQ6#	
AW36	GPIO46	RESUME	I	PCL1KRQ7#		PCIECLKRQ7#	
AW39	GPIO47	RESUME	I	PEG_A_CLKRQ#		PEG_A_CLKRQ#	
AG38	GPIO48	MAIN	I	SDATAOUT1	Pull-up to +3.3V and connect to P24-pin 10	FRONT_USB_DET#	
AG40	GPIO49	MAIN	O	SATA3GP	Pull-up to +3.3V and pull-down to GND. See PCA spec to determine the stuffing requirements for these resistors.	BRD_ID0	
AW5	GPIO50	MAIN	I	PCL1REQ#1	Use as REQ1#	REQ1#	
AK6	GPIO51	MAIN	O	PCL1GNT#1	Use as GNT1#	GNT1#	
AY4	GPIO52	MAIN	I	PCL1REQ#2	Pull-up to +3.3V	REQ2#	
BA9	GPIO53	MAIN	O	PCL1GNT#2	Connect to TP	GNT2#	
AW8	GPIO54	MAIN	I	PCL1REQ#3	Through a 8.2KΩ series resistor, connect to P14-pin 2 and pull-down to GND.	BOOT_BLK_EN#	
AW3	GPIO55	MAIN	O	PCL1GNT#3		GNT3#	
AW35	GPIO56	RESUME	I	PEG_B_CLKRQ#	Connect to circuit that controls the amplifier's output.	AUD_AMP_DIS#	
AL32	GPIO57	MAIN	I	PCH_GPI5	Pull-up to +3.3VSB	TPM_PP	
AY31	GPIO58	RESUME	O	SML1CLK		SML1CLK	
AT31	GPIO59	RESUME	I	OC0	Associated with USB port 0 powerwell. For ICH debug purposes, each USB OC# signal must be accessible for probing.	USB_OC#	
BA33	GPIO60	RESUME	O	SMLDALERT#		SMLDALARM	
AK31	GPIO61	RESUME	O	SUS_STAT#	Power Down for external TPM	LPCPD#	
AW31	GPIO62	RESUME	O	SUSCLK	SUSCLK to SIO	SUSCLK	
AW36	GPIO63	RESUME	O	SLP_S5#	Connect to USB Power Control on SIO	SLP_S5#	
AD10	GPIO64	MAIN	O	CLKOUTFLEX0		CLKOUTFLEX0	
AK1	GPIO65	MAIN	O	CLKOUTFLEX1		CLKOUTFLEX1	
AW6	GPIO66	MAIN	O	CLKOUTFLEX2		CLKOUTFLEX2	
AL3	GPIO67	MAIN	O	CLKOUTFLEX3		CLKOUTFLEX3	
AY34	GPIO72	RESUME	I	PCH_GPI2	Through a series 1KΩ resistor, pull-up to +3.3VSB and connect to P5-pin 10.	CHASSIS_ID1	
AW35	GPIO73	RESUME	I	PCIECLKRQ0#		PCIECLKRQ0#	
AY32	GPIO74	RESUME	O	SMLIALERT#		SMLIALERT#	
AR31	GPIO75	RESUME	O	SMLIDATA		SMLIDATA	

SIO9 PIN ASSIGNMENT (UPDATE PENDING)			
Pin	Pin Name	Function	Implementation
1	PWBTTN#	PWRBTN#	Connect to front panel header's power button pin
2	SLP_S3#	SLP_S3#	Connect to ICH10's SLP_S3# signal
3	SLP_S5#	S4_STATE#	Connect to ICH10's S4_STATE# signal
7	PDS_EN	CPU_FAN_TACH	Connect to the CPU fan tach interface
8	COLOR	LED_PWR_COLOR	Controls the Power LED color
10	PWBTOUT#	PWRBTN_OUT#	Connect to ICH PWRBTN# input
11	PS_ON#	PS_ON#	Connect to the appropriate power supply circuit
13	BLINK_GR	LED_PWR_BLINK	Connect to P5.2 through 68 ohm series resistor.
14	SIOPME#	RING#	Connect to ICH8 RI#
17	CLAMP_CTRL	CLAMP_CNTRL	Use for clamping PCA voltage rails to decrease rail decay time
28	SMB1SCL	SMB_CLK_MAIN	Connect to the clock signal of the main powered system SMBus
29	SMB2SCL	SMB_CLK_STDBY	Connect to the clock signal of the standby powered system SMBus
33	GPRST2#	PCI_EXP_RST#	Use to reset all the PCIe devices and slots
34	FANPWM2	CHAS_FAN_PWM	Connect to the Chassis Fan PWM interface
35	GPIQ25	PWM_IN	Connect to the ICH10's PWM0 output - NEW for Eaglelake
36	PME_IN#	P_PME#	Connect to the PME# pin of the ICH10
37	USB_PWR#	USB_PWR#	Input to USB Power control; connect to the ICH10's SLP_S5# signal
38	3V_SW_MAIN#	3V_DUAL_CNTRL	Connect to control inputs of dual rail switches
39	EVENT6#	PCI_EXP_WAKE#	Connect to WAKE# pins of PCIe devices and slots
47	PDS_EN2	PDS_EN2	Use as control signal for appropriate voltage regulators
48	CPU_FRSNT1#	SKTOCC#	Connect to SKTOCC# on CPU
49	WAKE_OUT#	ICH_WAKE#	Connect to the ICH10's WAKE# input
50	GPIE14	HOOD_LOCK#	Connect to P124 pin 1 and a 2.2K pull-up to +5V.
51	GPIOE16	HOOD_UNLOCK#	Connect to P124 pin 6 and a 2.2K pull-up to +5V.
53	AUDIO_BEEP	DIAG_BEEP	Connect to the system's integrated audio solution
54	FANPWM1	CPU_FAN_PWM	Connect to the CPU fan's PWM circuit
55	GPIO35	PECT1 REQ#	Connect to the ICH10's BM_BUSY# signal - New for Eaglelake; C#/C4 support
56	HD_LED_IN#	SATA_LED#	Connect to the ICH10's SATA_LED# output signal
58	HMSCL	HLTH_MON_CLK	Connect to CLK pin on SensorBus device
59	HMSDA	HLTH_MON_DAT	Connect to DAT pin on SensorBus device
60	GPIOE10	FLPY_DRV DEN	Use in floppy implementation
61	HD_LED_OUT#	HD_LED#	Connect to the front panel HDD LED
100	SMB1SDA	SMB_DATA_MAIN	Connect to the data signal of the main powered system SMBus
101	SMB2SDA	SMB_DATA_STDBY	Connect to the data signal of the standby powered system SMBus
102	5V_USB_MAIN#	5V_USB_MAIN#	Connect to the control pin of the 5V_DUAL circuit.
103	GPIOE41	PS_FAN_TACH	Where applicable, connect to power supply's fan tach circuit.
104	FANPWM3	PS_FAN_PWM	Where applicable, connect to the power supply's fan PWM circuit
105	PWRGD_01	PWRGD_30MS	Use for appropriate system board sequencing
106	PWRGD_02#	PWRGD_30MS#	Use for appropriate system board sequencing
110	FAN_TACH4	CHAS_FAN_TACH	For systems with a chassis fan, connect to the chassis fan TACH circuit
111	SMI#	LPC_SMI#	Connect to appropriate ICH10 SMI-capable GPIO; reference ICH10 GPIO matrix
120	RI2#	RI2#	Where applicable, connect to appropriate serial port pin
122	DCD2#	DCD2#	Where applicable, connect to appropriate serial port pin
123	SIN2	SIN2	Where applicable, connect to appropriate serial port pin
124	SOULT2	SOULT2	Where applicable, connect to appropriate serial port pin
125	DSR2#	DSR2#	Where applicable, connect to appropriate serial port pin
126	RTS2#	RTS2#	Where applicable, connect to appropriate serial port pin
127	CTS2#	CTS2#	Where applicable, connect to appropriate serial port pin
128	DTR_BOUT2#	DTR2#	Where applicable, connect to appropriate serial port pin




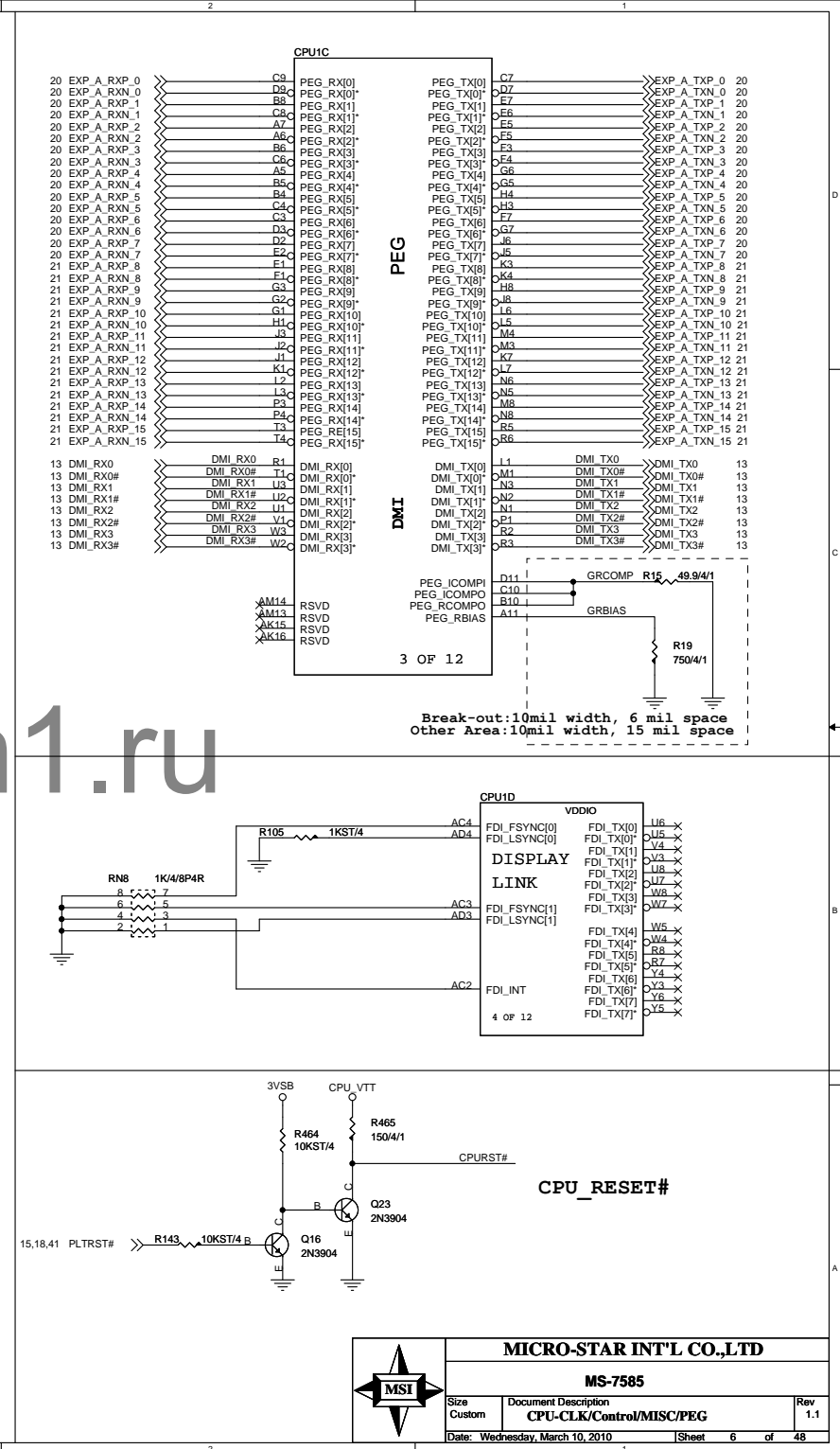
MICRO-STAR INT'L CO.,LTD

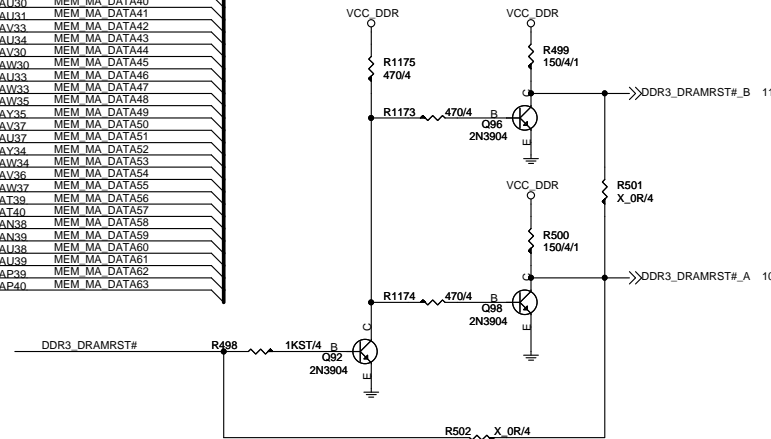
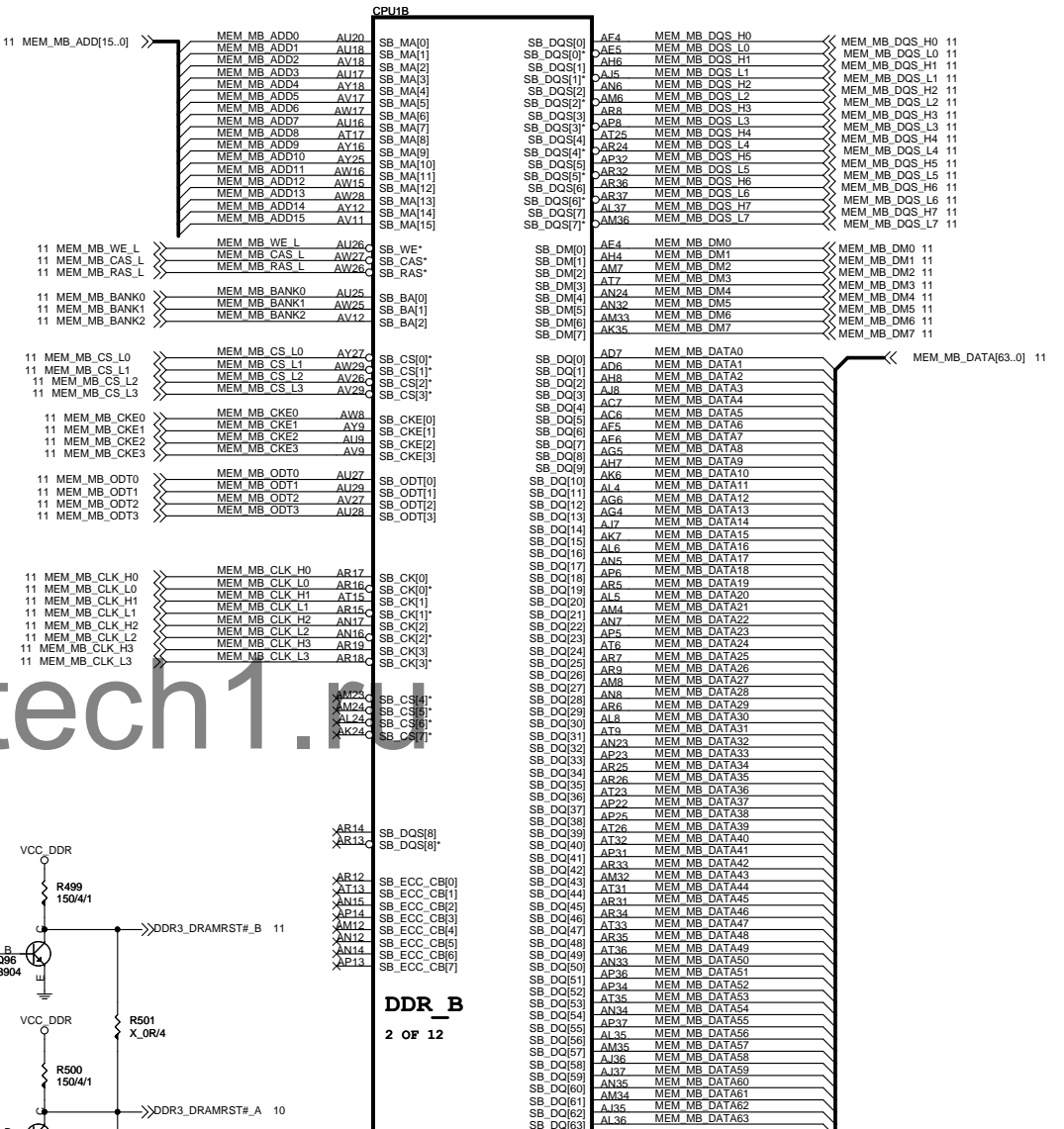
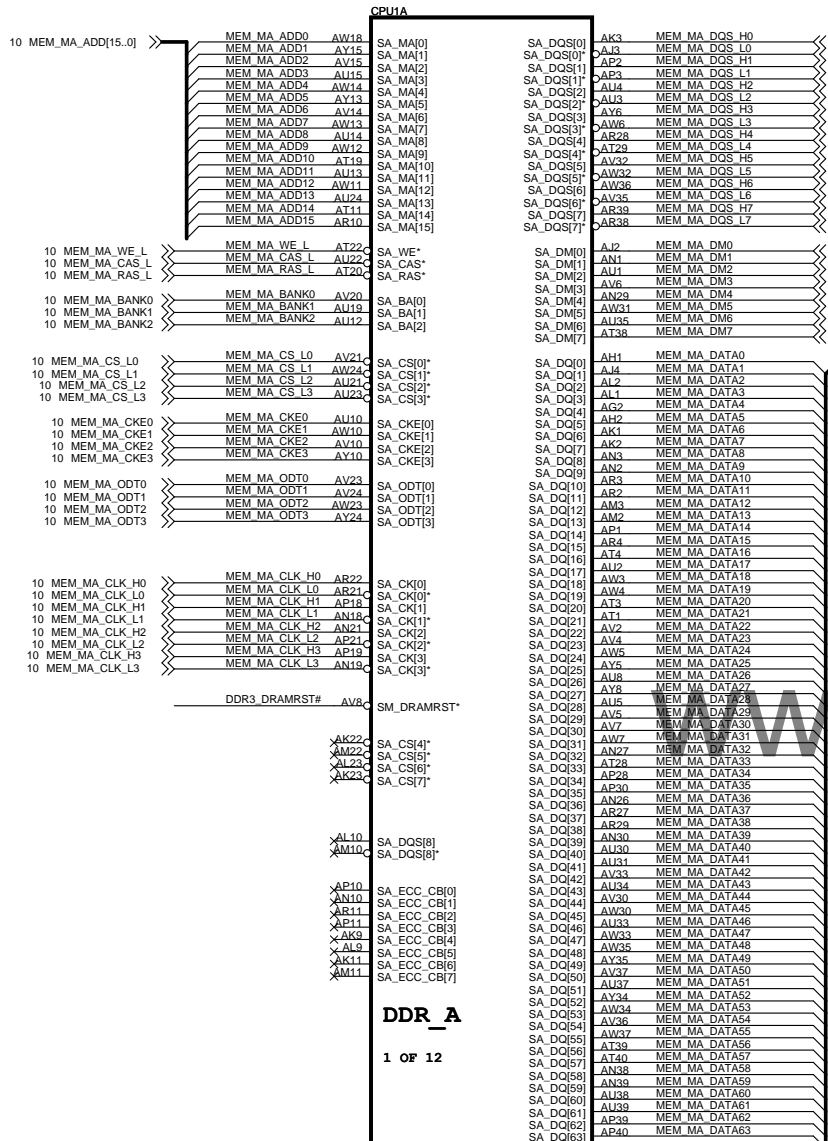
MS-7585

Size	Document Description	Rev
Custom	GPIO Table	1.1
Date: Wednesday, March 10, 2010		Sheet 4 of 48

www.aitech1.ru

			MICRO-STAR INT'L CO.,LTD	
			MS-7585	
Size Custom	Document Description Clock Distribution			Rev 1.1
Date: Wednesday, March 10, 2010		Sheet	5	of 48

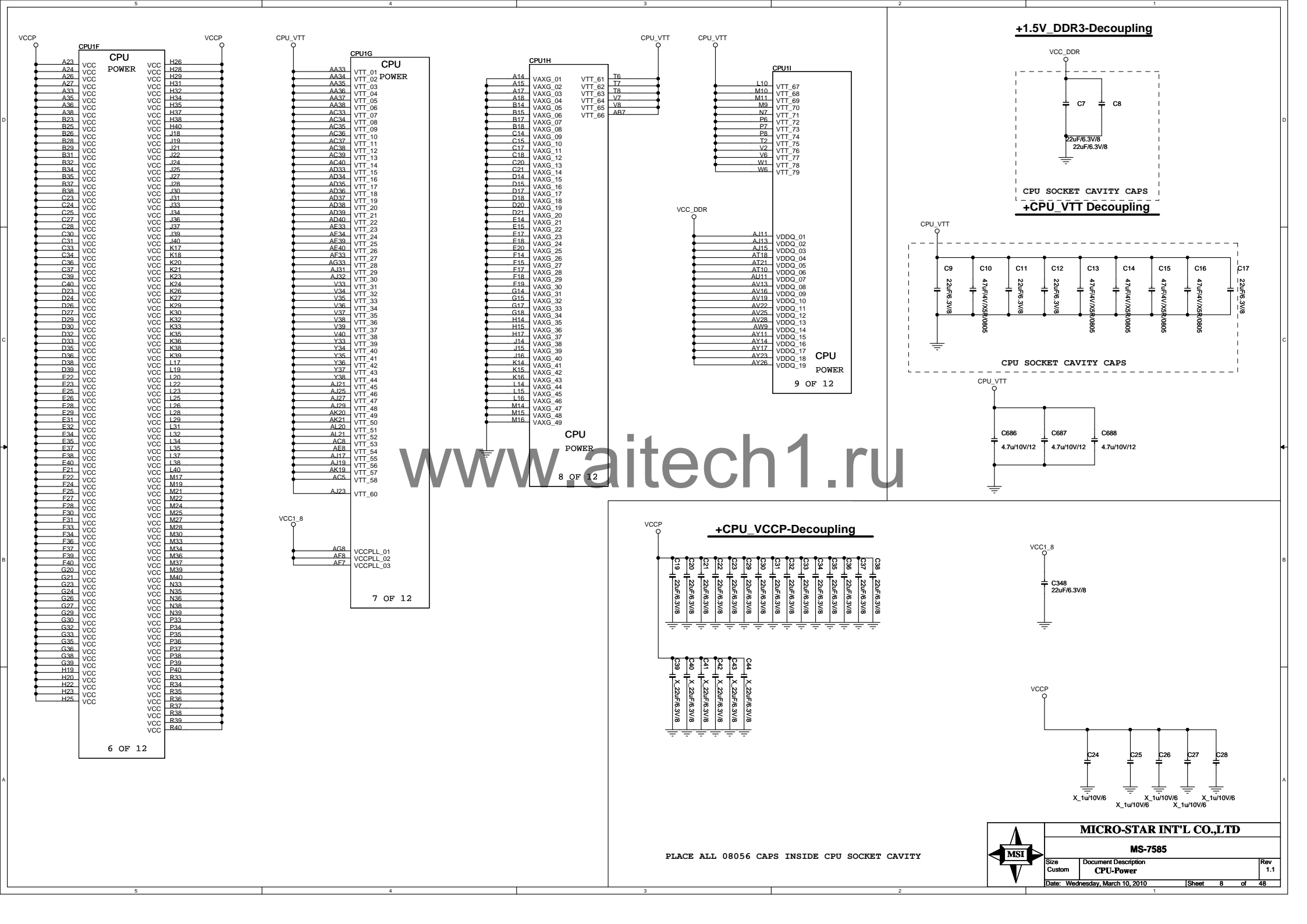




MICRO-STAR INT'L CO.,LTD

MS-7585

Size	Document Description	Rev
Custom	CPU-Memory	1.1
Date: Wednesday, March 10, 2010	Sheet 7 of 48	

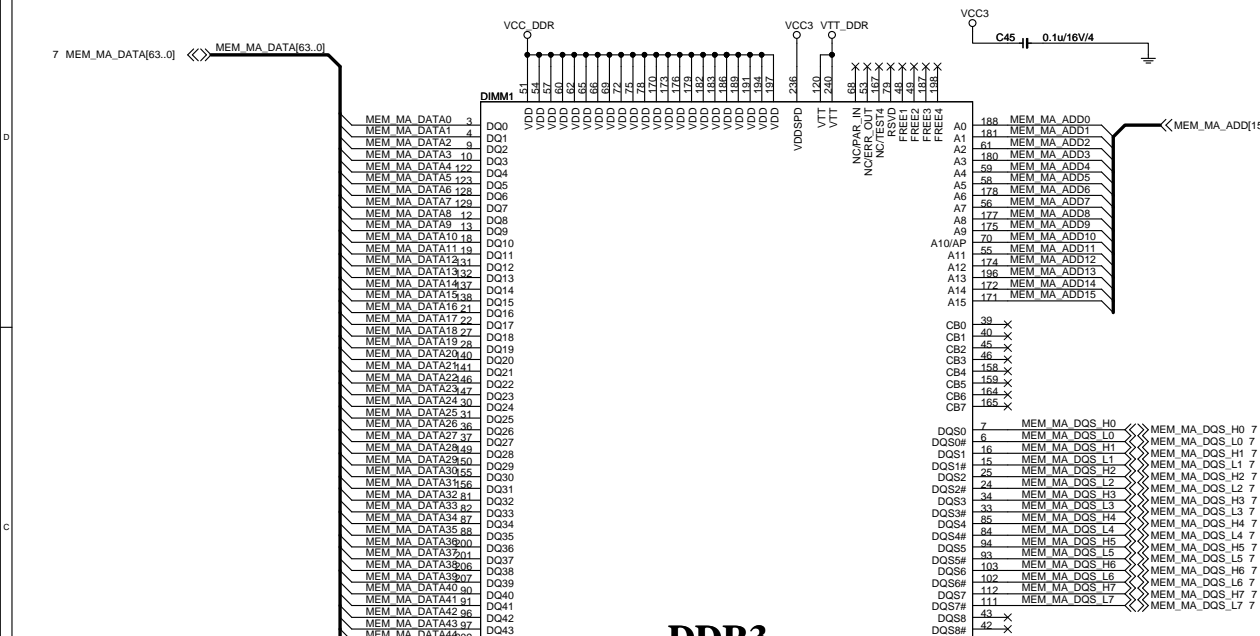




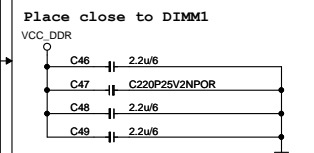
FOLLOW DDR3 DIMM VREFDQ Platform Design
Guide Change Option 3



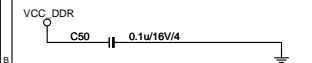
DDRIII DIMM_A1



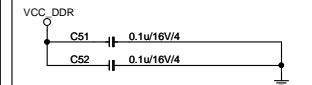
DDR3



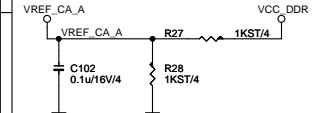
Place close to DIMM1 with DIMM2



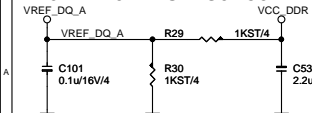
Place close to DIMM2



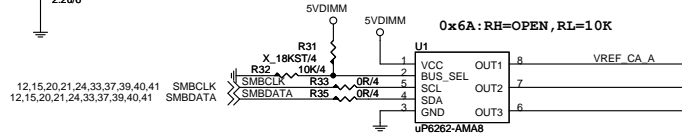
UPI VOLTAGE CONSOLE



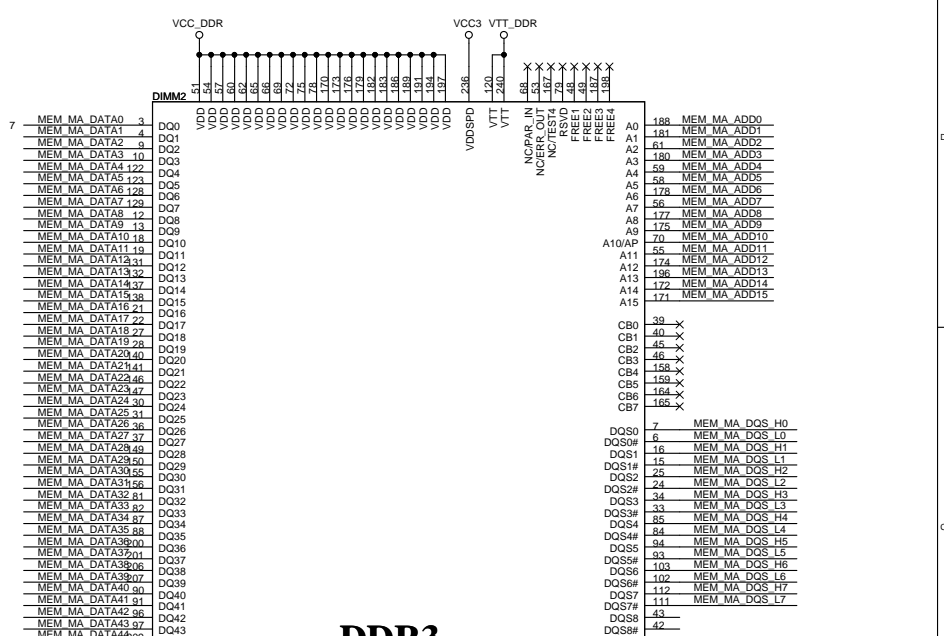
UPI VOLTAGE CONSOLE



UPI VOLTAGE CONSOLE (3+1)



DDRIII DIMM_A2



DDR3

[illegible]

20	VSS	BA0	MEM MA BANK1
23	VSS	BA1	MEM MA BANK2
26	VSS	BA2	
29	VSS	73	MEM MA WE L
32	VSS	WE#	MEM MA RAS L
35	VSS	RAS#	MEM MA CAS L
38	VSS	CAS#	DDR3 DRAMRST# A
41	VSS	RESET#	

44	VSS		184	MEM_MA_CLK_H2	MEM_MA_CLK_H2_7
47	VSS	CK0	185	MEM_MA_CLK_L2	MEM_MA_CLK_L2_7
80	VSS	CK0#	63	MEM_MA_CLK_H3	MEM_MA_CLK_H3_7
83	VSS	CK1(NU)	64	MEM_MA_CLK_L3	MEM_MA_CLK_L3_7
		CK1#(NU)			

[illegible]

MICRO-STAR INT'L CO.,LTD

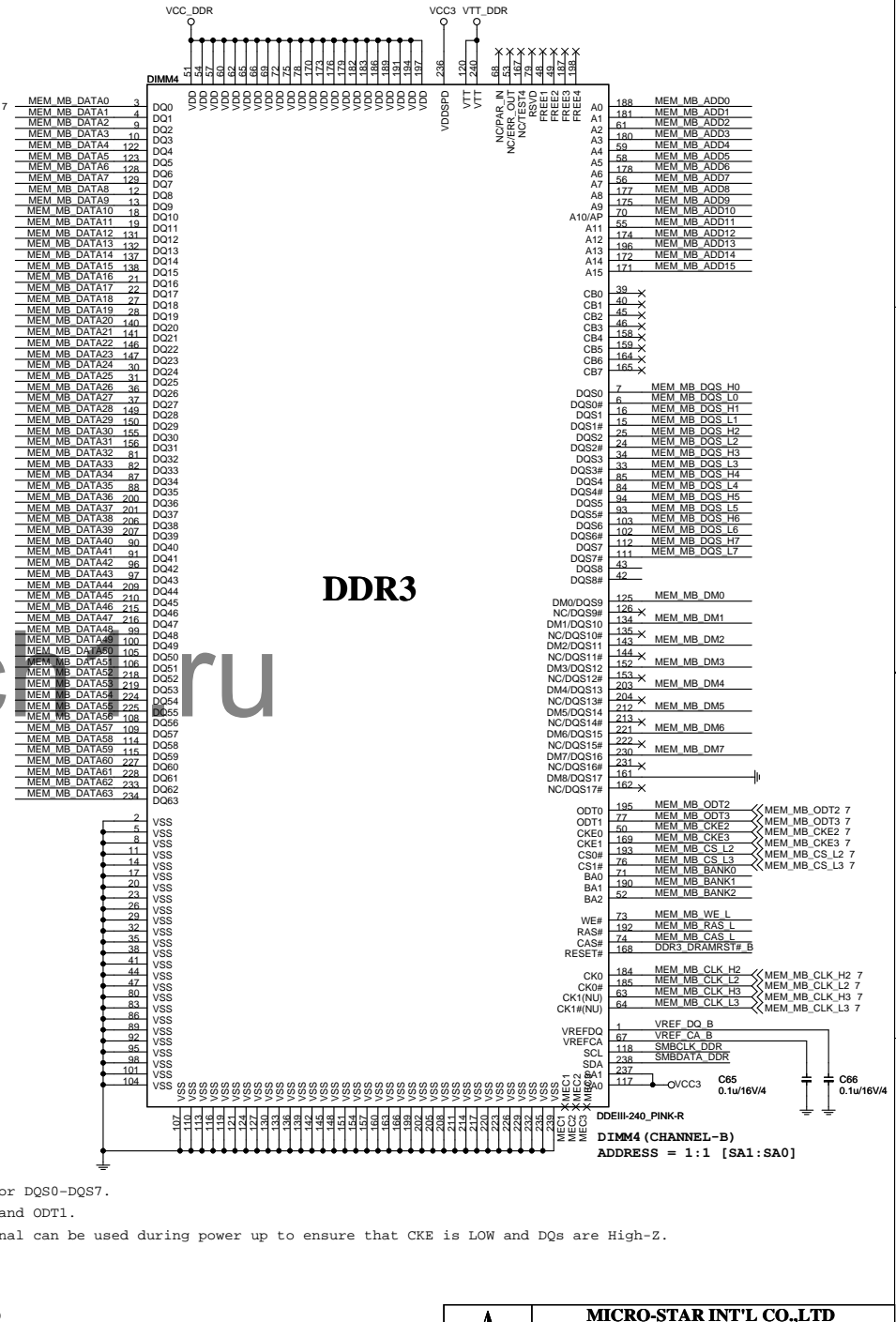
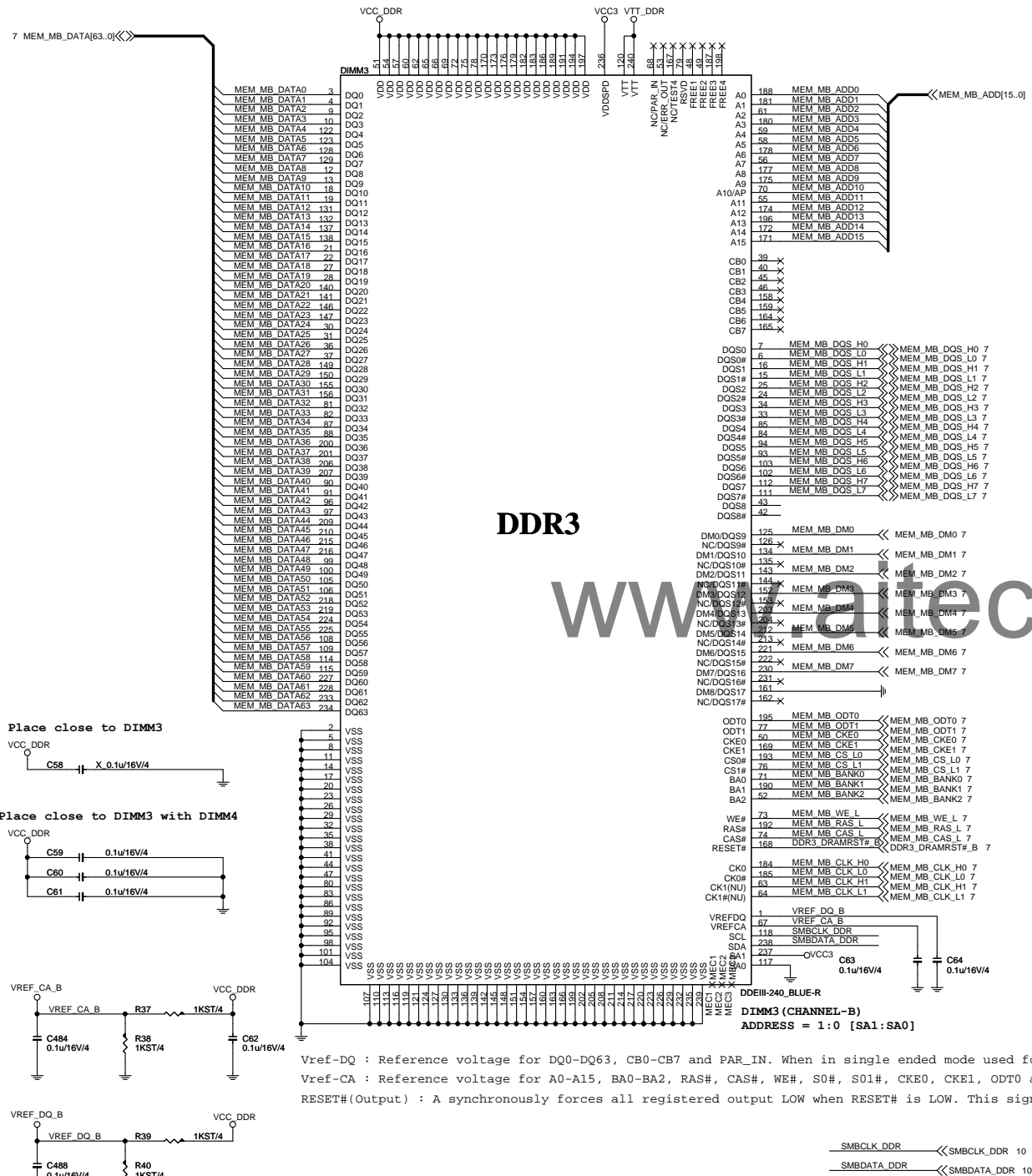
MS-7585

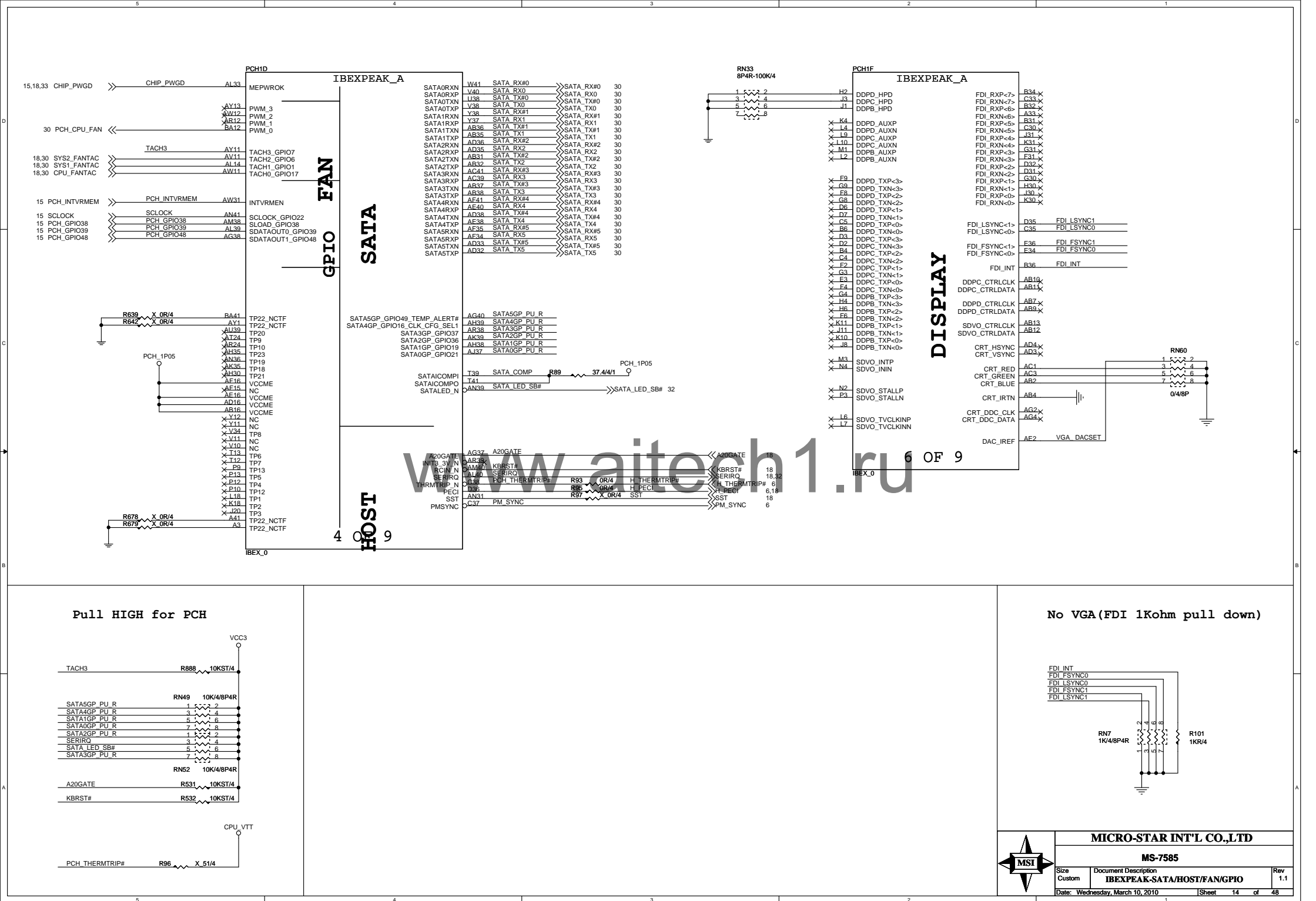
Size Custom	Document Description DDR III DIMM 1 / DIMM 2	Rev 1.1
----------------	--	------------

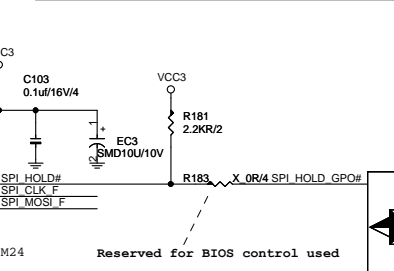
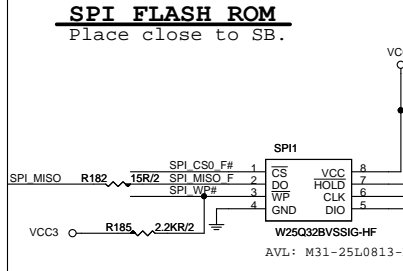
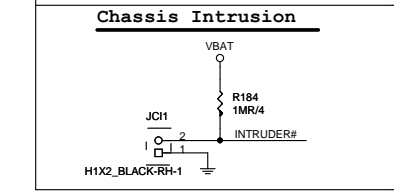
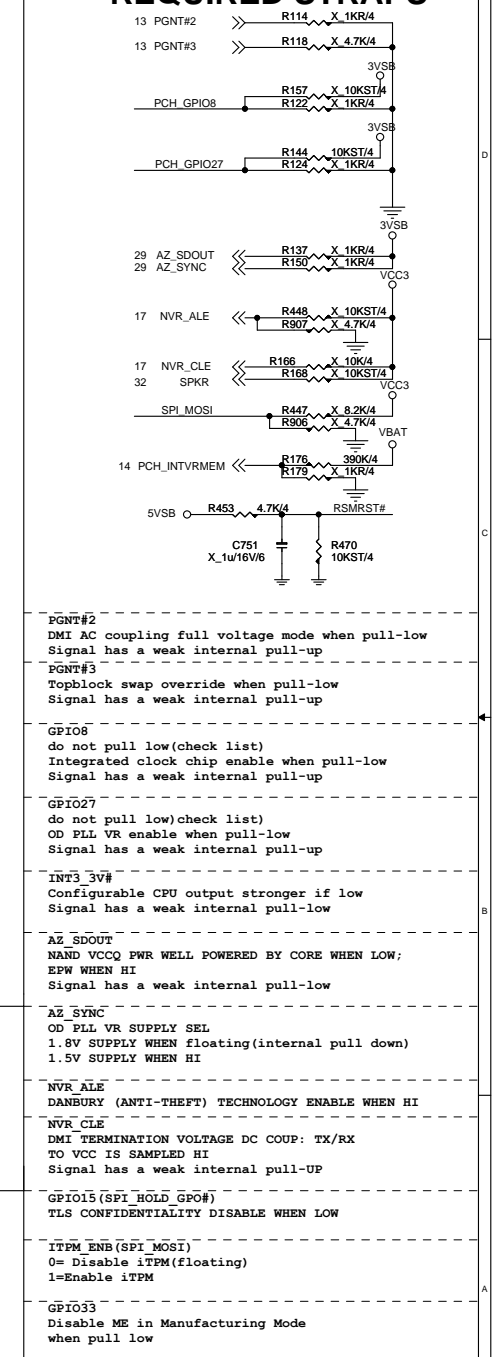
Date: Wednesday, March 10, 2010	Sheet 10 of 48
---------------------------------	----------------


DDR3 DIMM_B1

DDR3 DIMM_B2







	MICRO-STAR INT'L CO.,LTD		
	MS-7585		
	Size Custom	Document Description IBEXPEAK-SMB/LPC/AUDIO/RTC	Rev 1.1
	Date: Wednesday, March 10, 2010		Sheet 15 of 48

PCH_1P05

L1
X_1uH/50mA/0.4Ohm/8

VCCFIDPLL

C105
X_10uF/6.3V/X5R/8

R186 X_0R/8

VCCACLK

C106
X_10uF/6.3V/X5R/8

C107
X_1u/6.3V/4

R187 X_0R/8

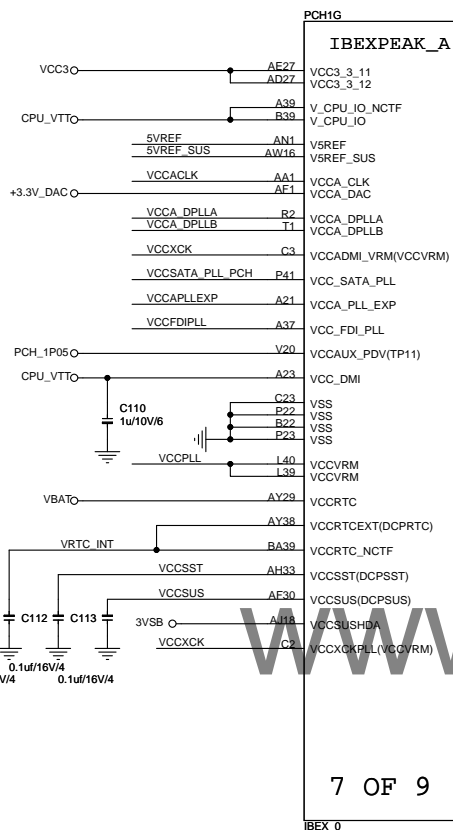
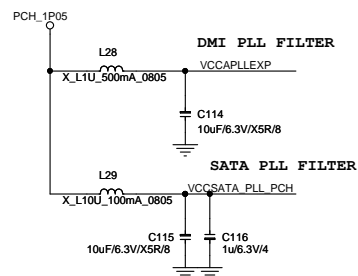
VCC_A_DPLL_A

C108
X_1u/6.3V/4

R188 X_0R/8

VCC_A_DPLL_B

C109
X_1u/6.3V/4



VCC3

+3.3V DAC

R193 0R/6

C18 0.1uF/6V/4

Near ball AF1

PCH_1P05 VCC1

R197 0R/4

R198 0R/4

VCC1_B0 VCCXCK

PCH_1P05 VCC1

R202 0R/4

R198 0R/4

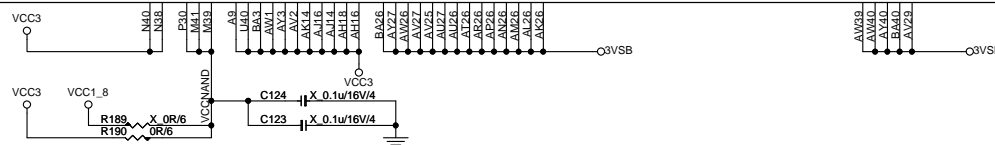
VCCPLL

[illegible]

POWER

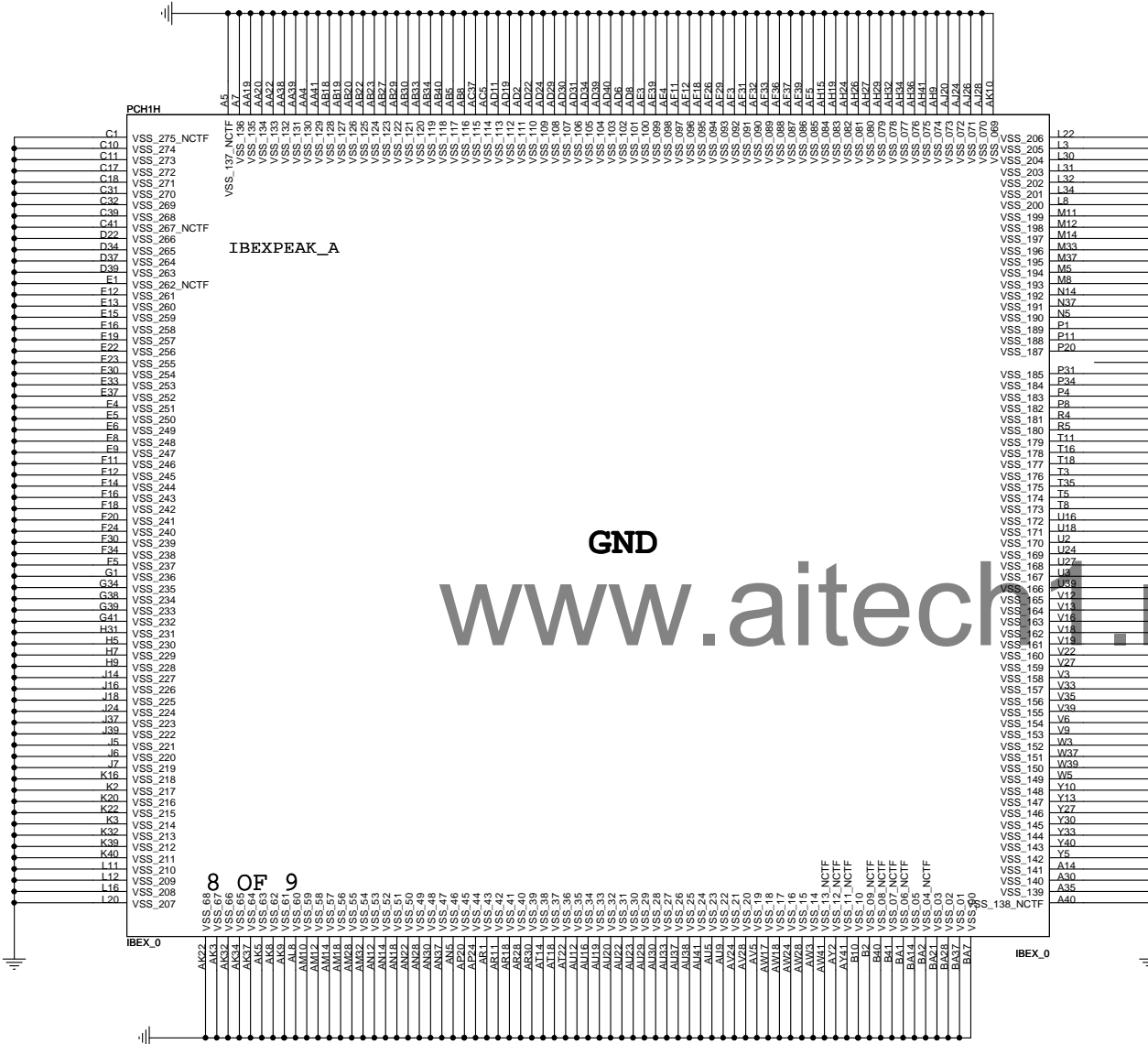
VCCS1(DCPS1)
AF30 VCCSUS(DCPSUS)
A118 VCCSUSHDA
C2 VCCXOKPULL(VCCORM)

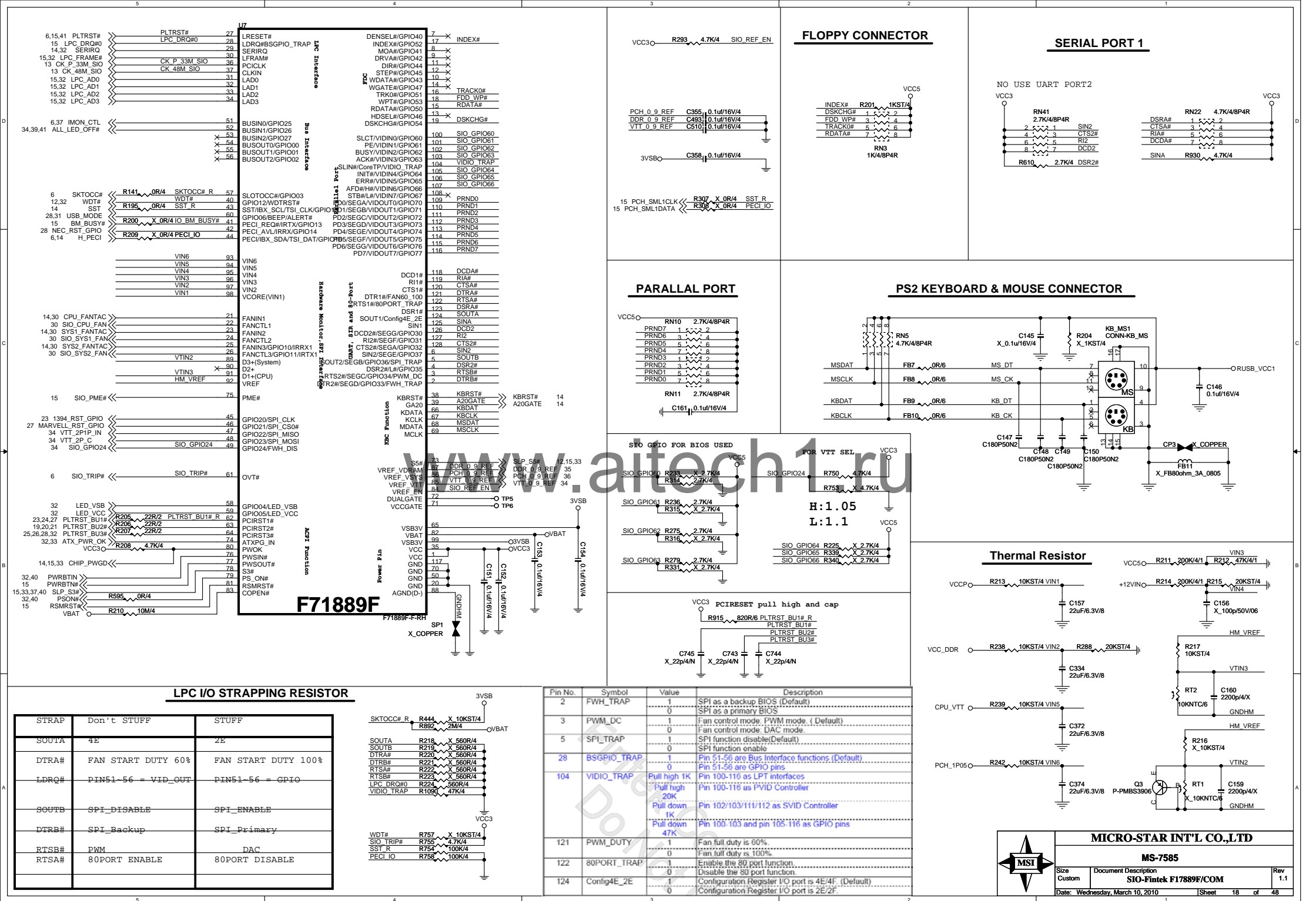
7 OF 9

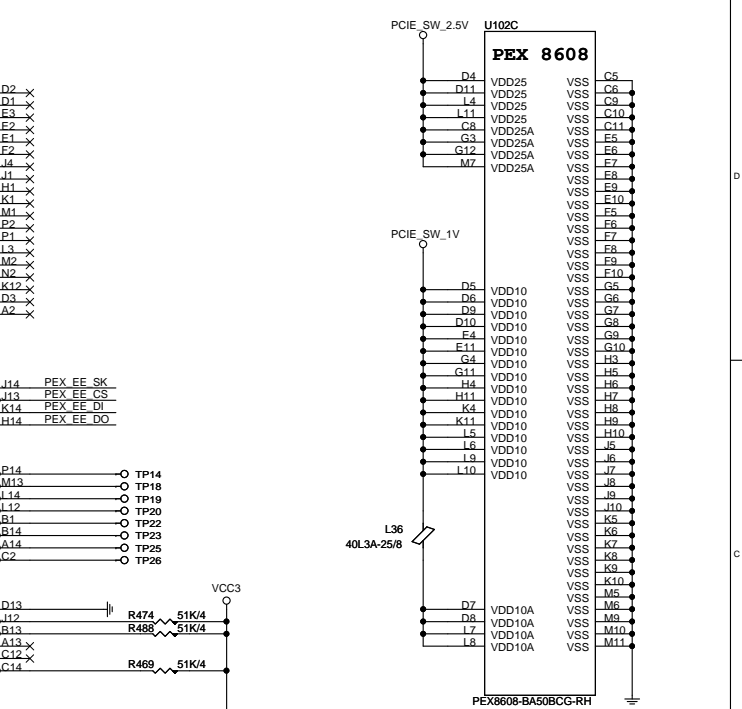
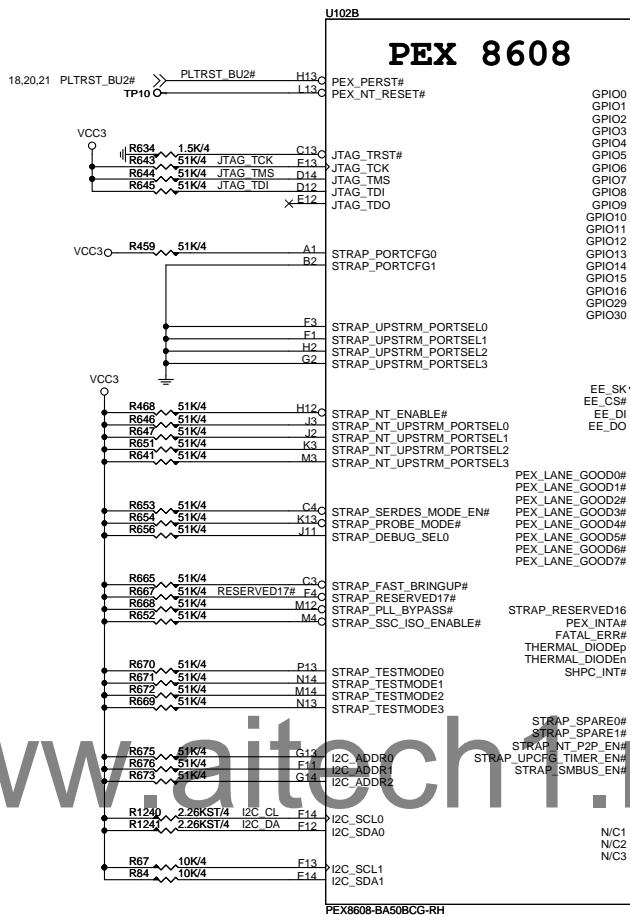
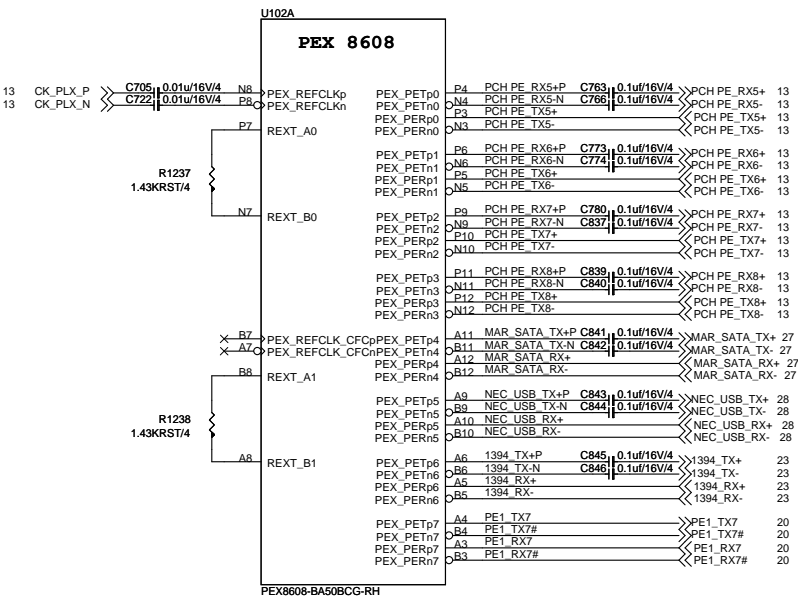


MS-7585

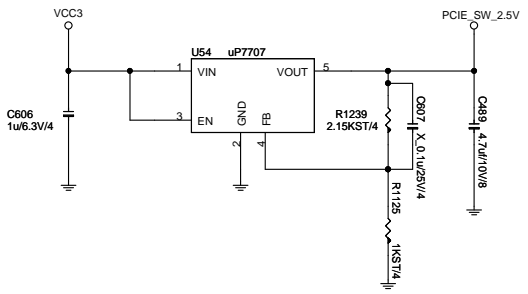
Size Custom	Document Description IBEXPEAK-POWER	Rev 1.1
Date: Wednesday, March 10, 2010		Sheet 16 of 48



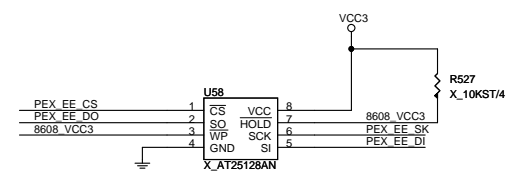




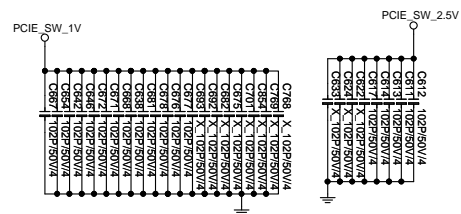
PCIE_SW_2.5V 0.05A



EEPROM



CAP



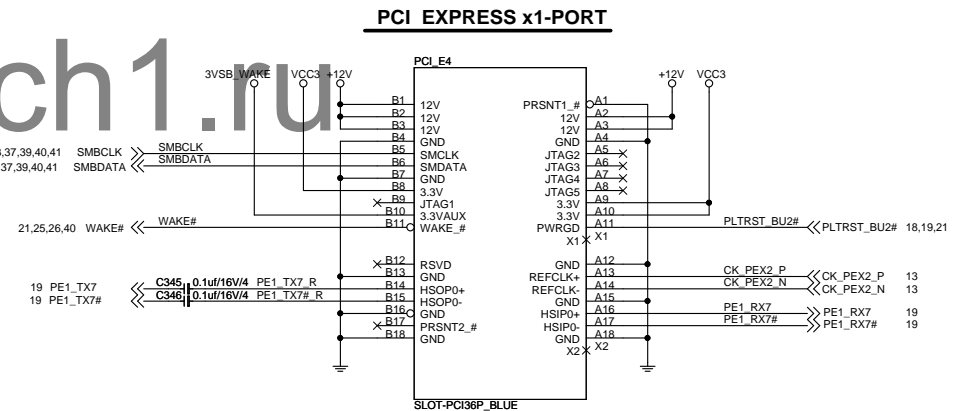
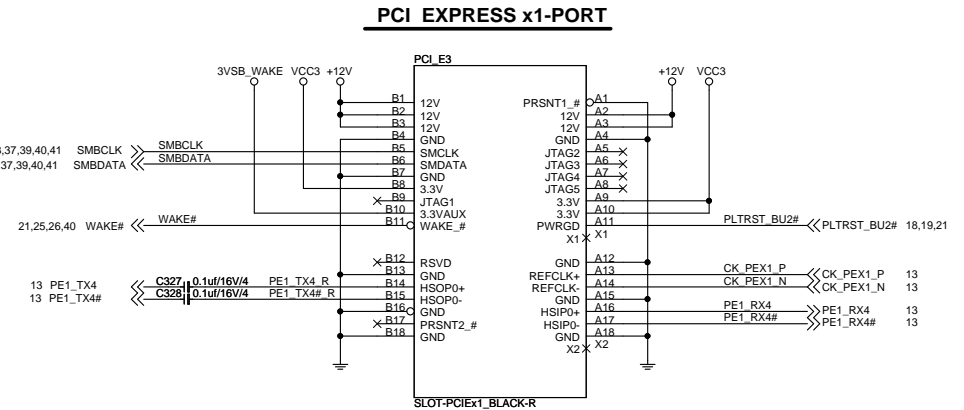
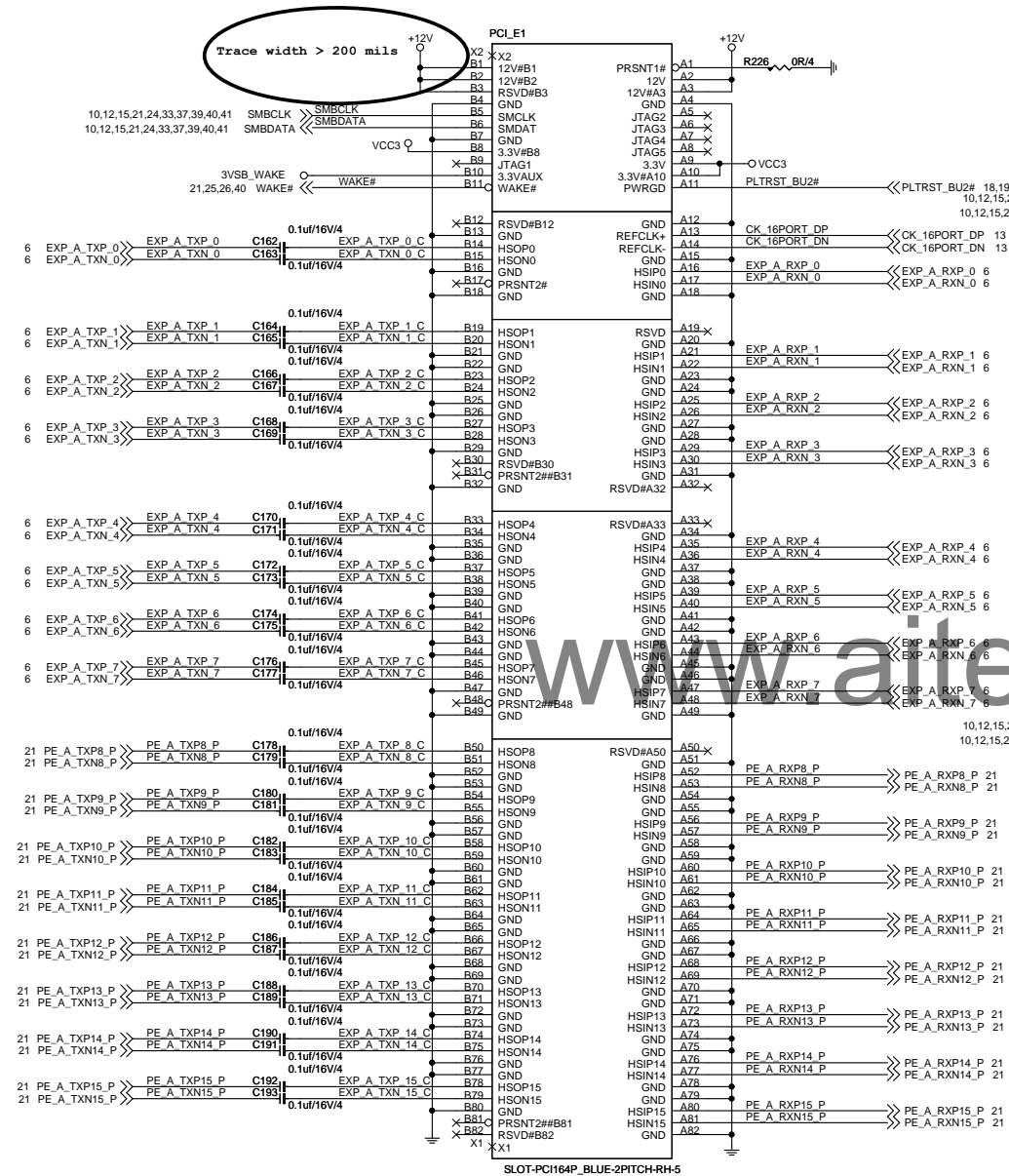
MICRO-STAR INT'L CO.,LTD

MS-7585

Size Custom Document Description **PLX8608** Rev 1.1

Date: Wednesday, March 10, 2010 Sheet 19 of 48

PCI Express X16 Slot

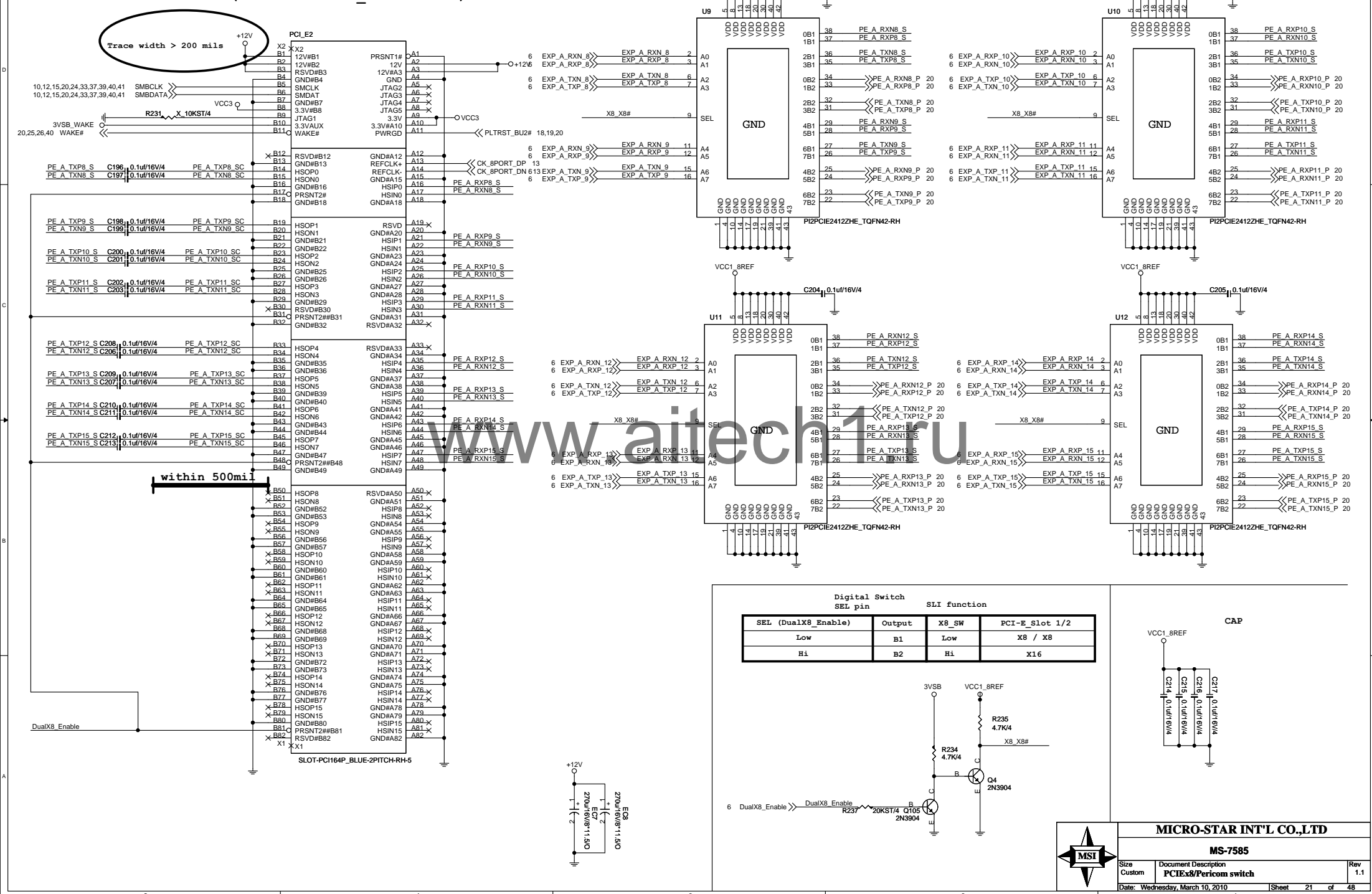


MICRO-STAR INT'L CO.,LTD

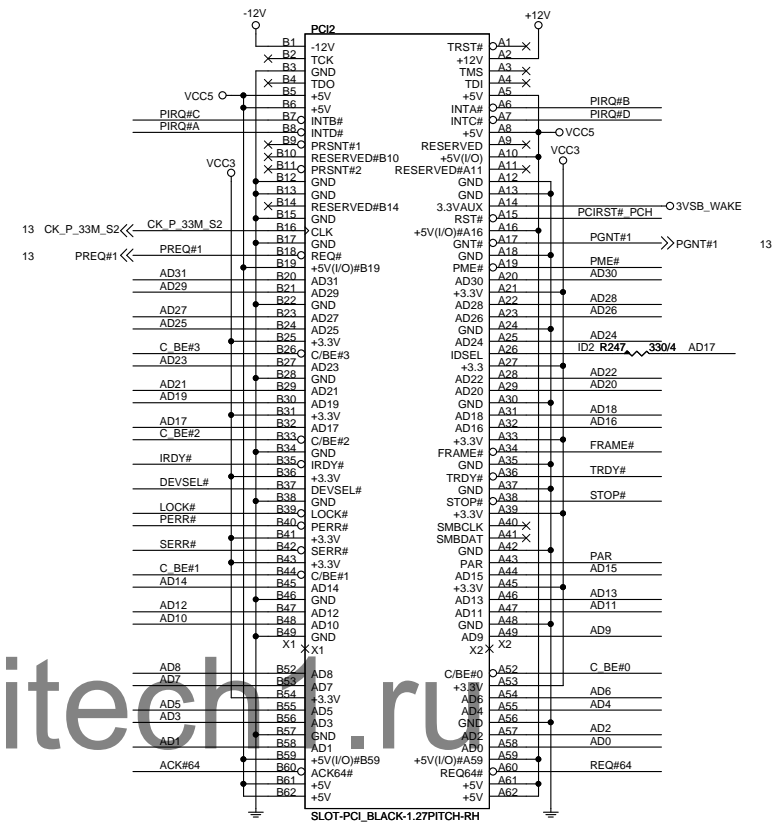
MS-7585

Size Custom	Document Description PCIE x16 & x1 Slots	Rev 1.1
Date: Wednesday, March 10, 2010		Sheet 20 of 48

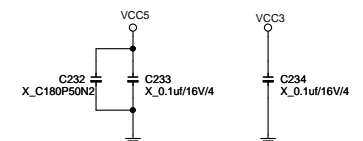
PCI Express X8 Slot
(Share with PCI E x16 Slots)



PCI SLOT 2 (PCI VER: 2.2 COMPLY)



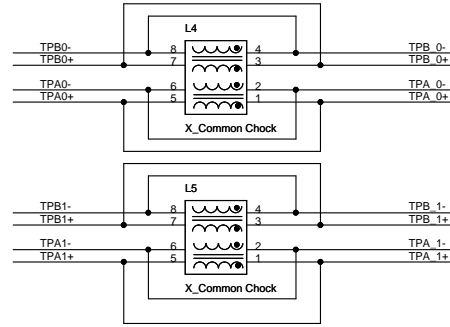
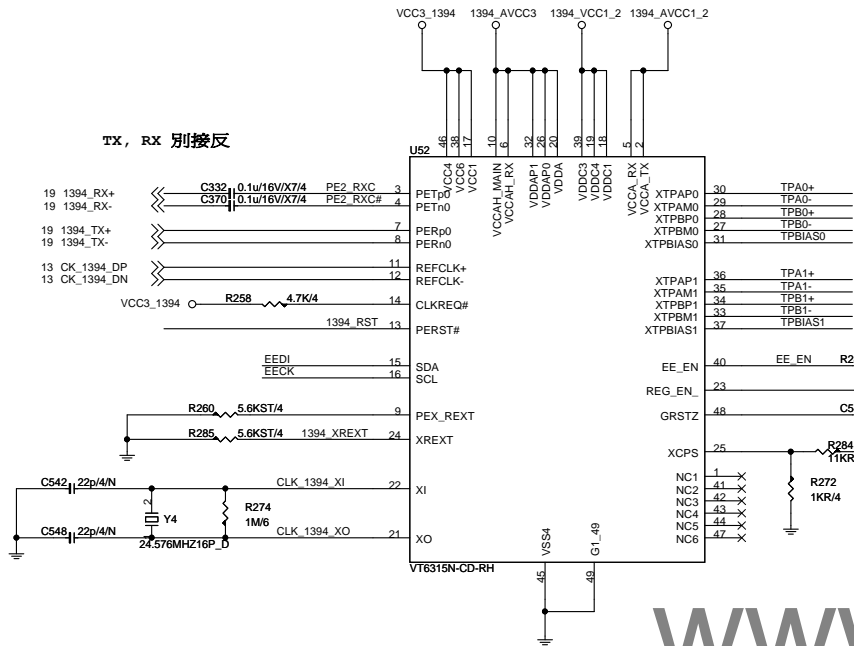
```
IDSEL = AD17
MASTER = PREQ#1
PIRQ#B
```



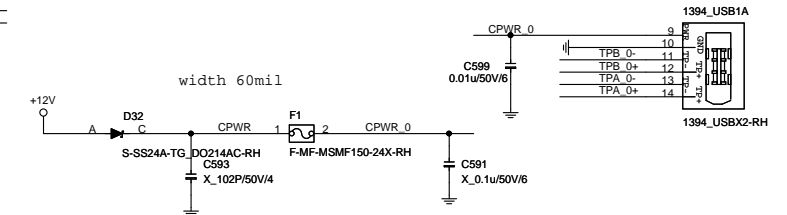
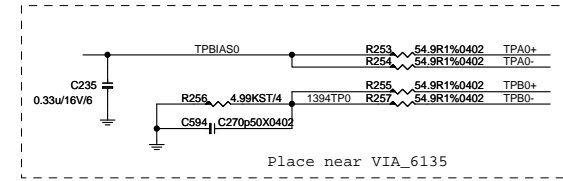
MS-7585

Size Custom	Document Description PCI Slot 1 & 2	Rev 1.1
Date: Wednesday, March 10, 2010		Sheet 22 of 48

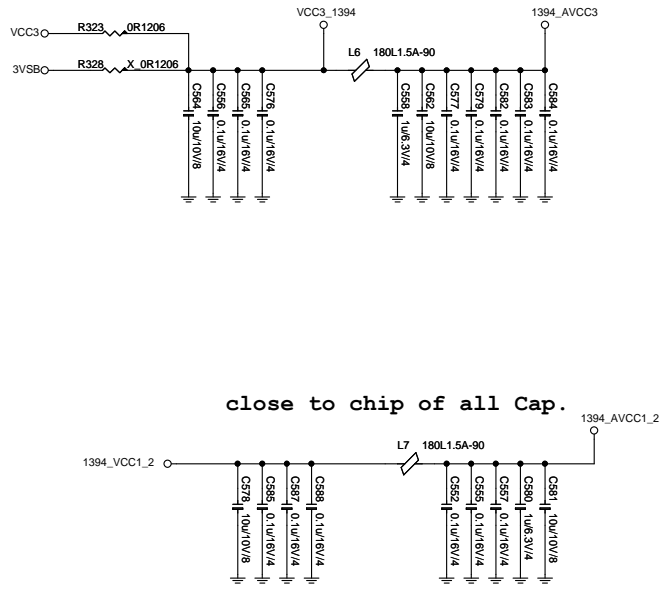
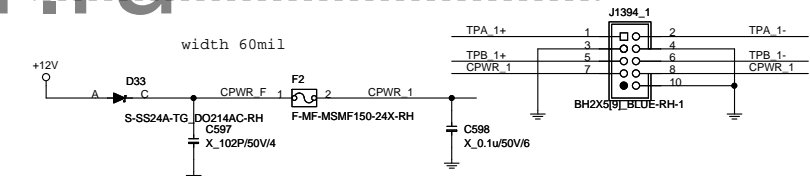
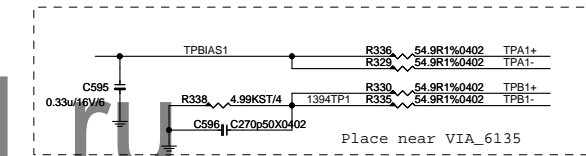
1394 CONTROLLER



Rear 1394 port

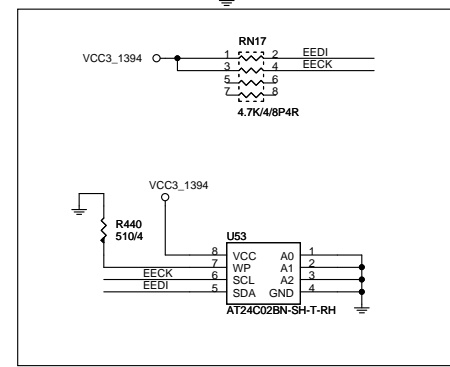
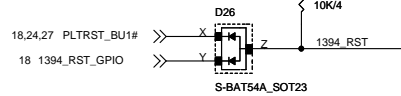


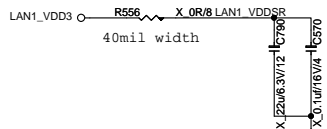
Front 1394 pin header



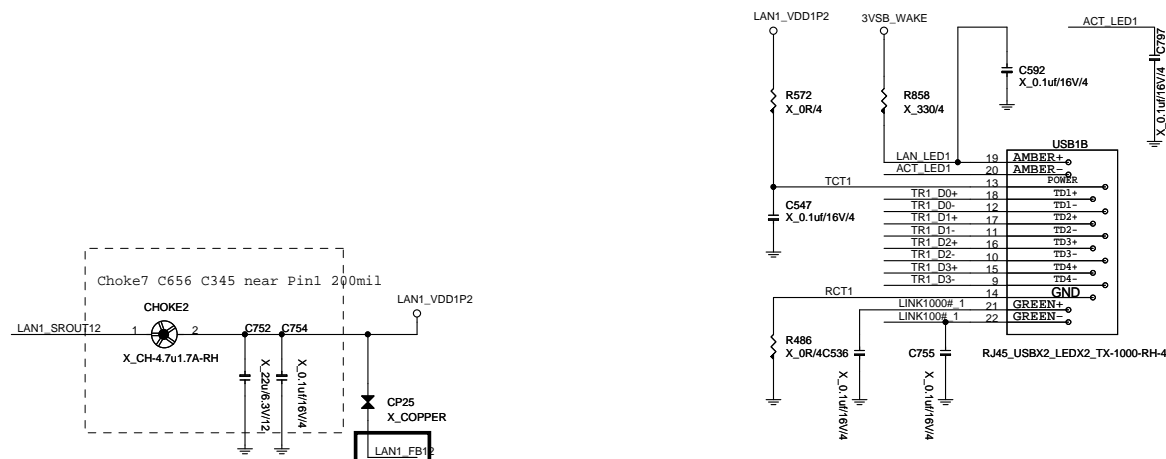
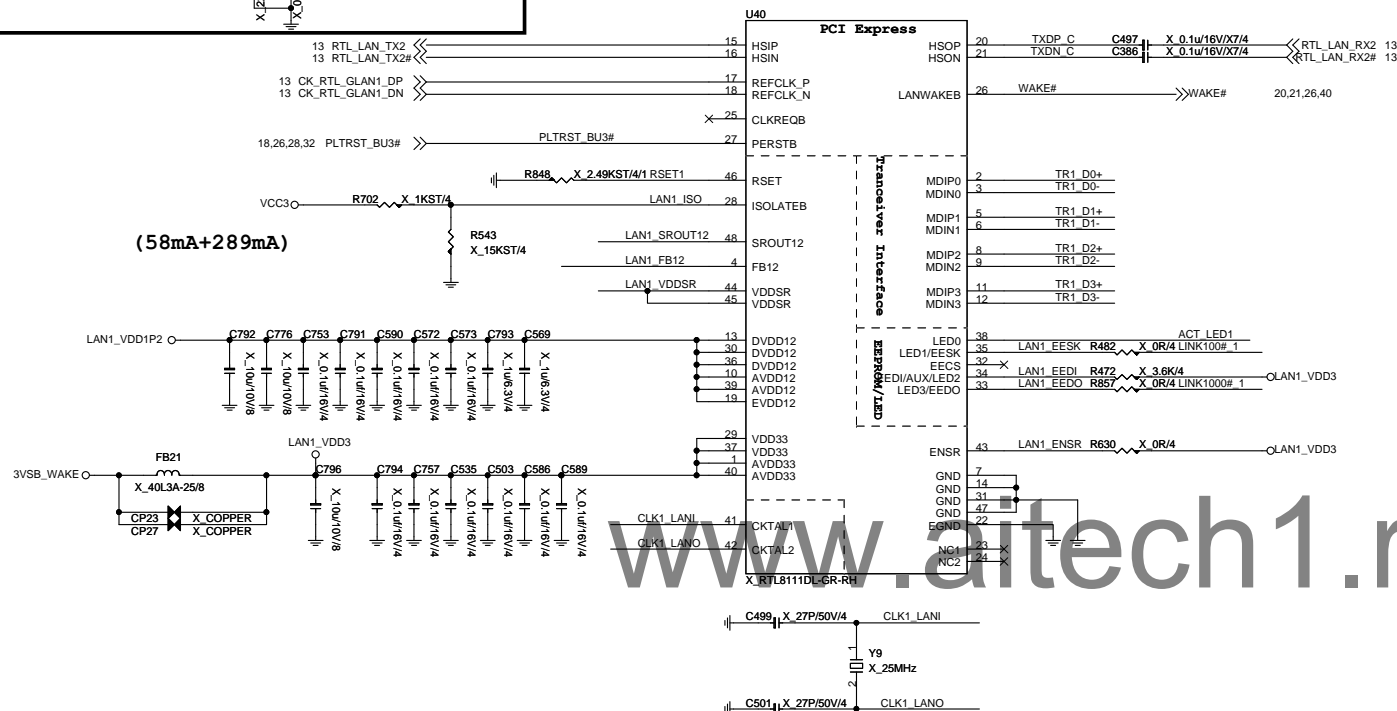
close to chip of all Cap.

close to chip of all Cap.

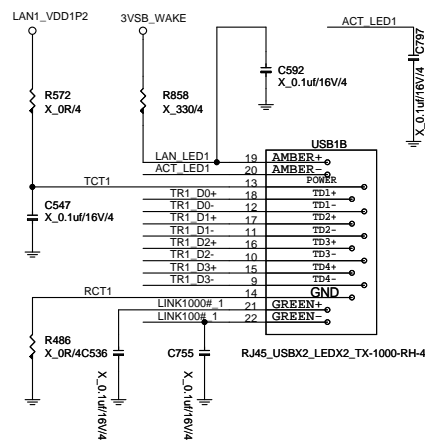




TX and RX 別接反





"FB12": A trace front CHOKE to RTL8111C pin5





Giga-Lan
N58-22F0181-S42

Link	Yellow
Active	Blinking
1000	Orange
100	Green
10	None

19 —  Yellow

20 —  Yellow

21 —  Orange

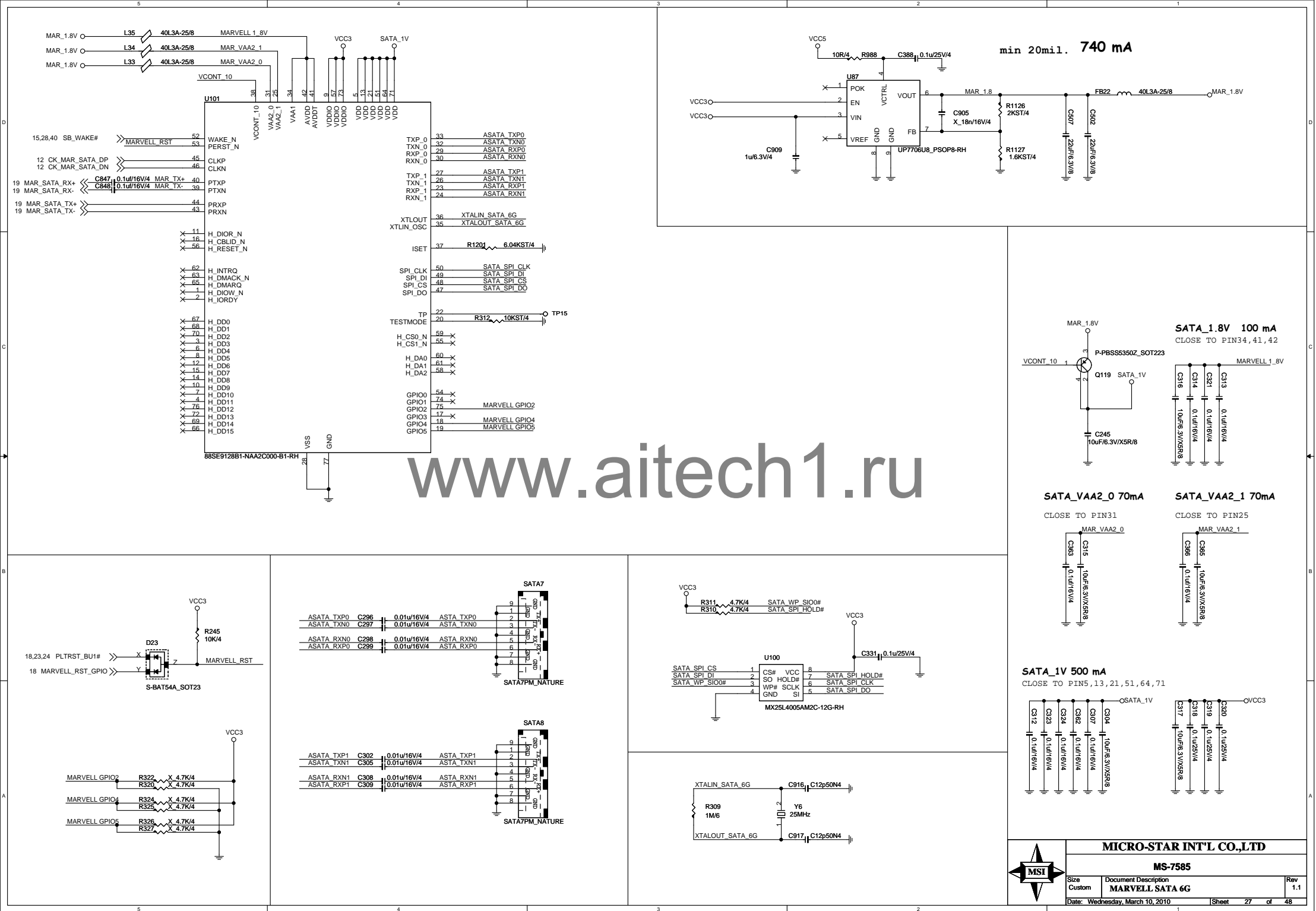
22 —  Green

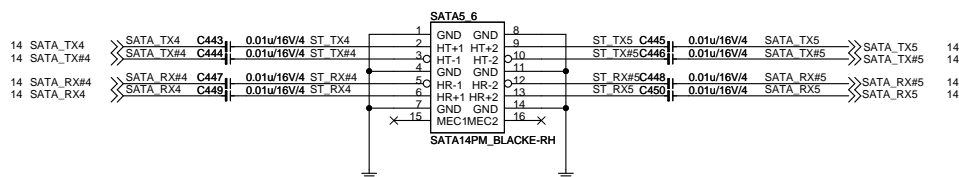
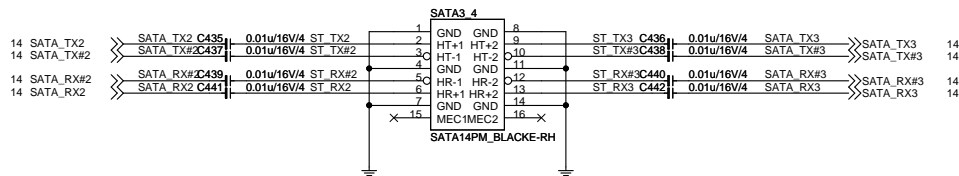
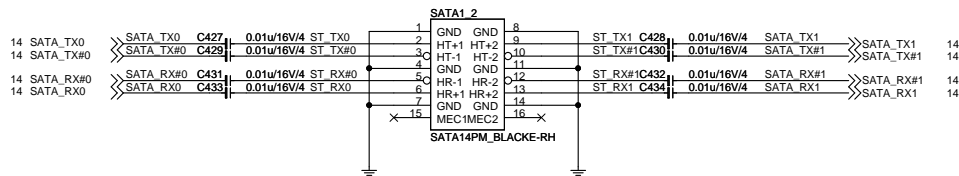


MICRO-STAR INT'L CO.,LTD

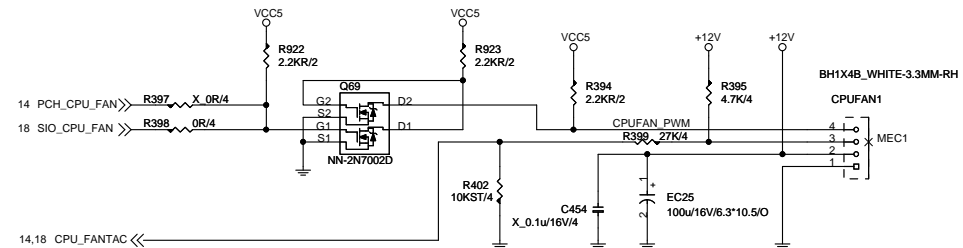
MS-7585

Size Custom	Document Description LAN - RTL8111DL-1	Rev 1.1
Date: Wednesday, March 10, 2010		Sheet 25 of 48



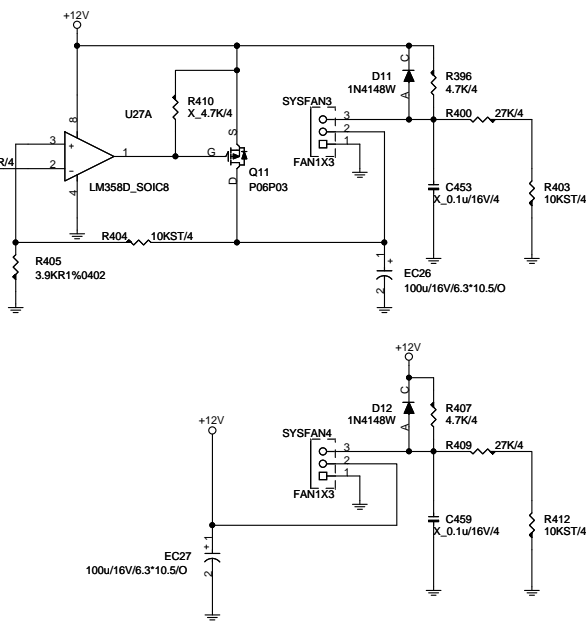
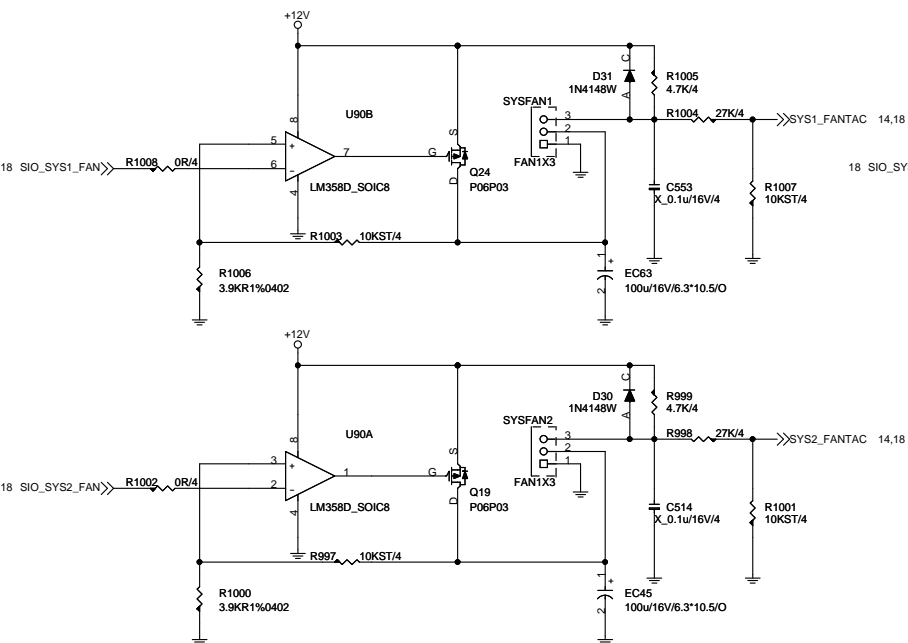


CPU FAN-COUNTROL CIRCUIT



www.aitech1.ru

FAN-COUNTROL CIRCUIT

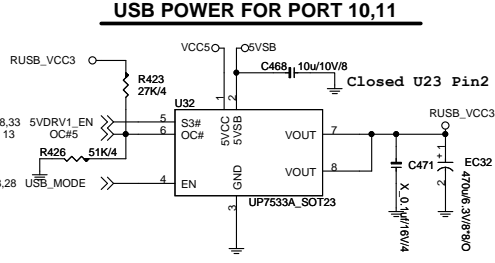
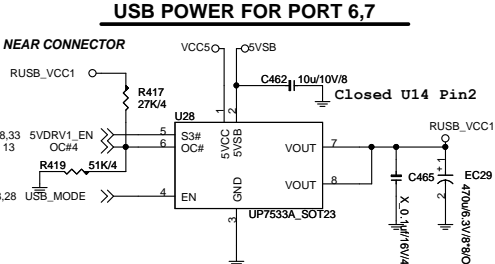


MICRO-STAR INT'L CO.,LTD

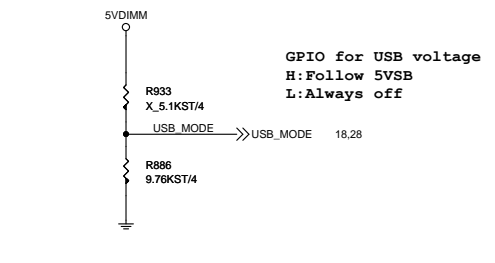
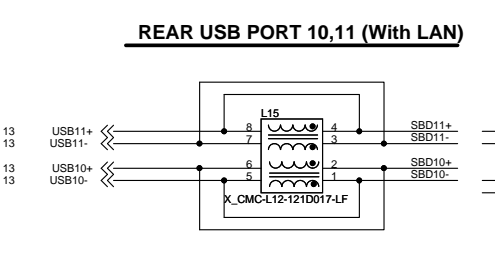
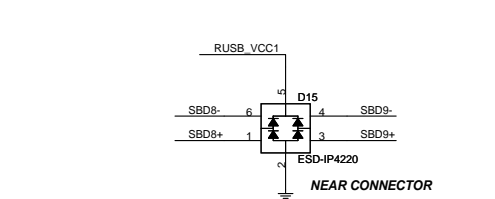
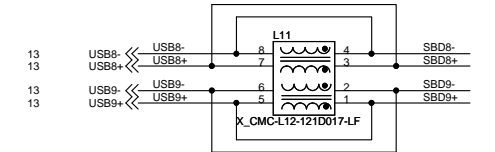
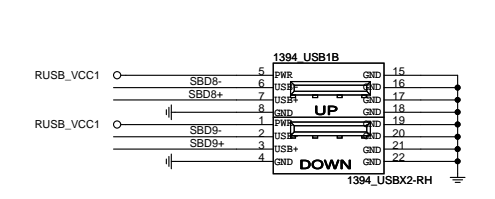
MS-7585

Size	Document Description	Rev
Custom	SATA & e-SATA Ports and Fan Control	1.1
Date: Wednesday, March 10, 2010	Sheet 30 of 48	

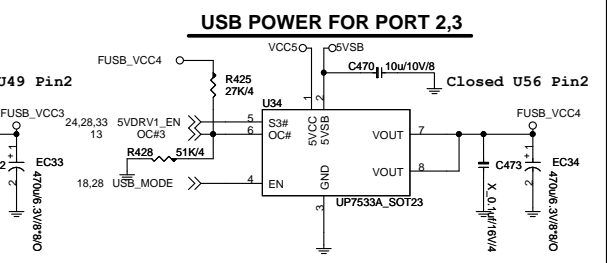
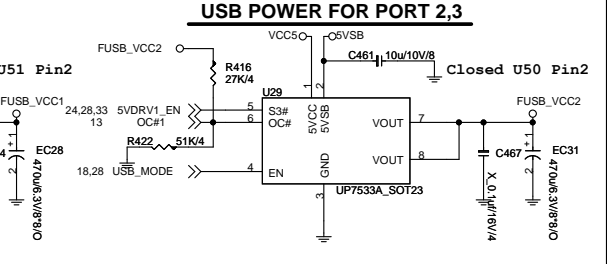
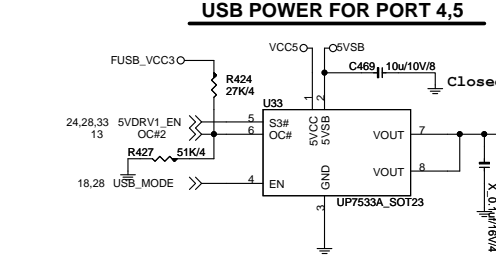
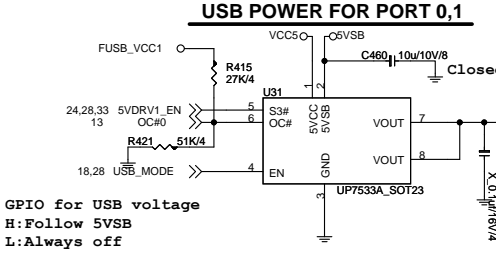
Rear USB Connector



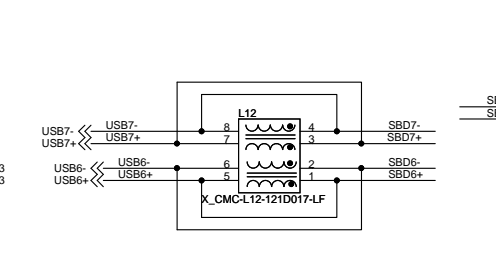
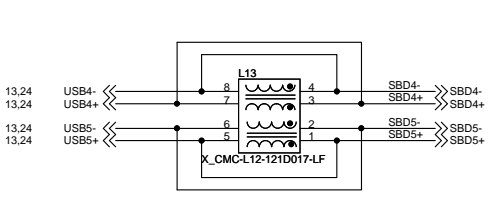
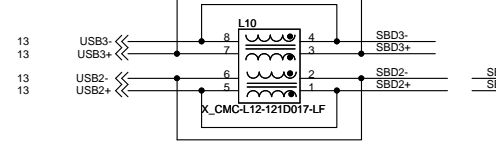
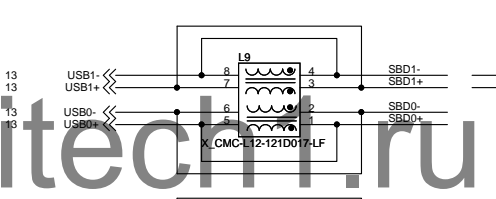
REAR USB PORT 6,7,8,9 (2x2)



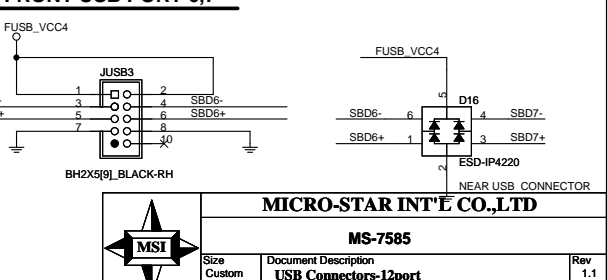
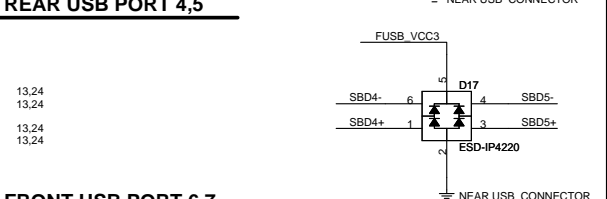
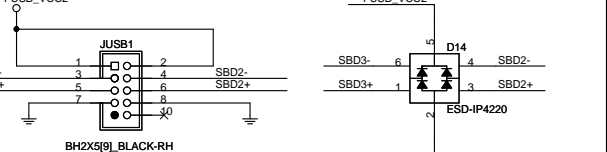
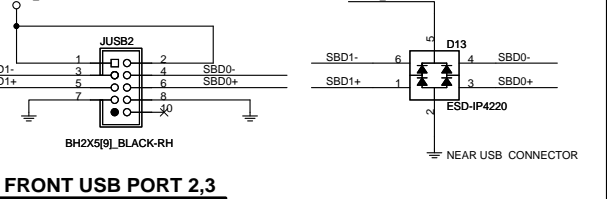
Front USB Connector



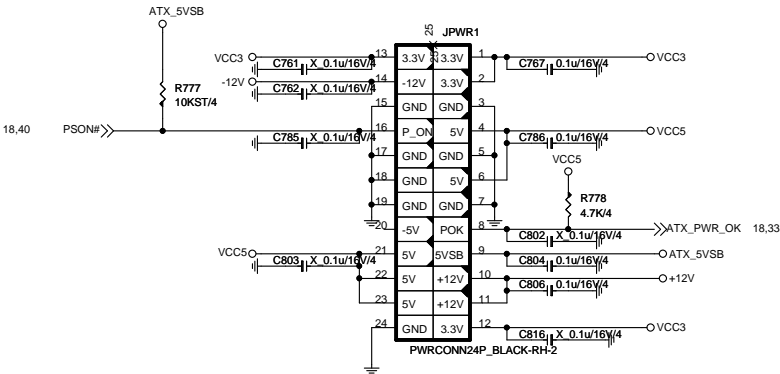
FRONT USB PORT 0,1



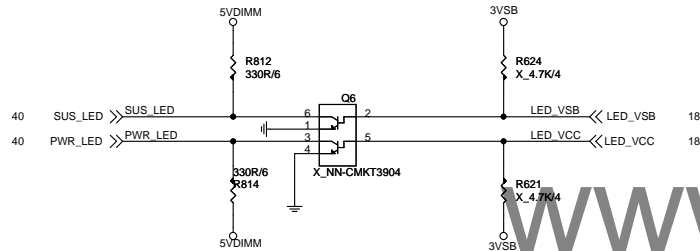
FRONT USB PORT 2,3



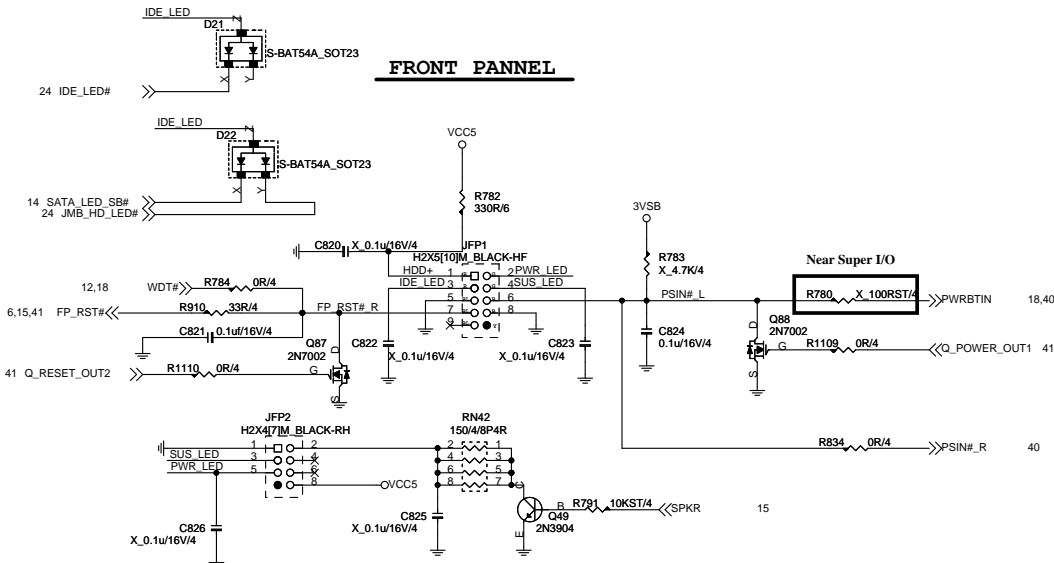
ATX POWER CONNECTOR



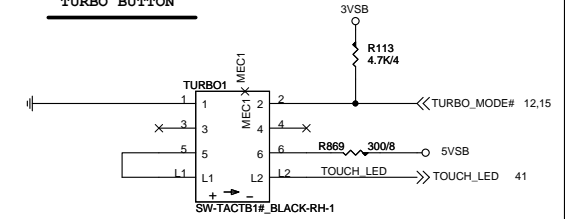
POWER LED Control



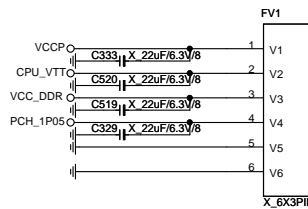
FRONT PANNEL



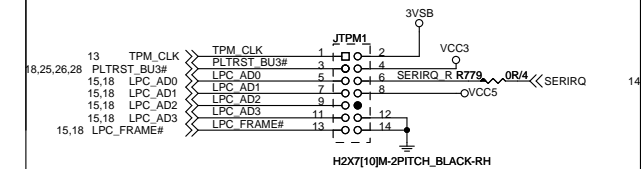
TURBO BUTTON



電壓測點



TPM

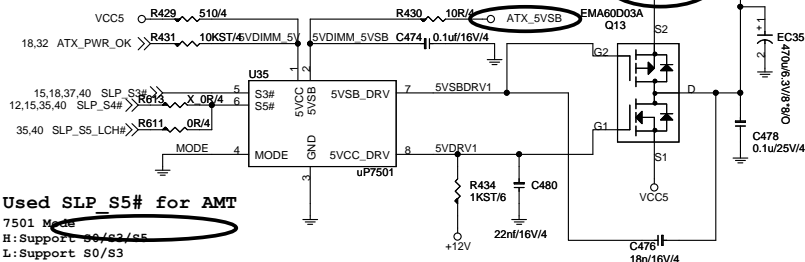


MICRO-STAR INT'L CO.,LTD

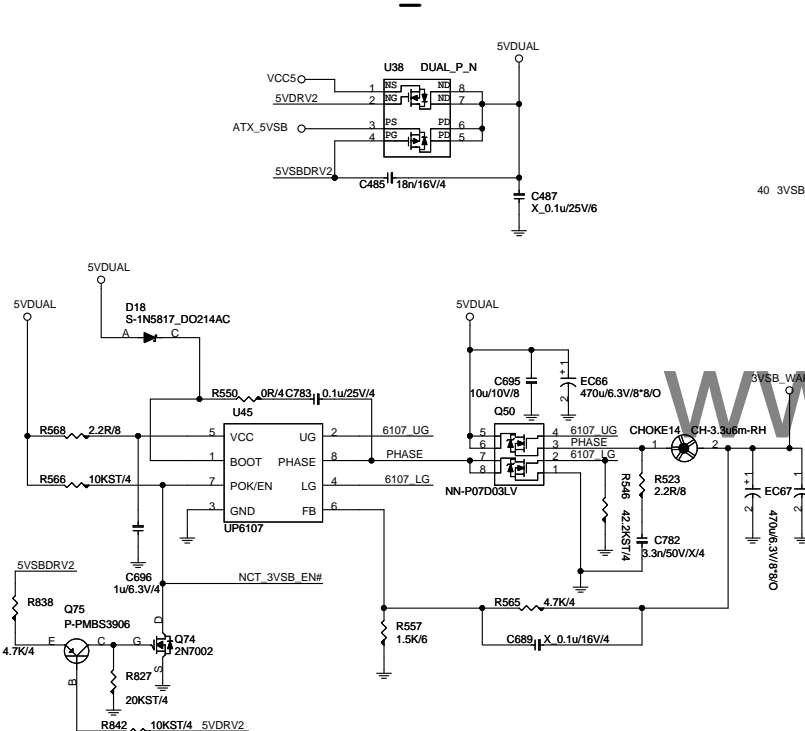
MS-7585

Size	Document Description	Rev
Custom	ATX PWR-Connector & Front Panel & EMI	1.1
Date: Wednesday, March 10, 2010	Sheet 32 of 48	

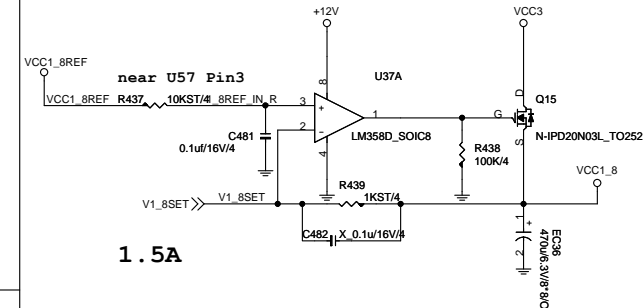
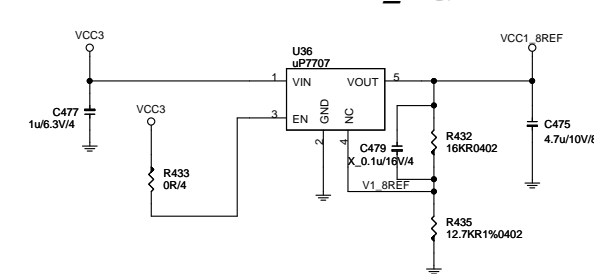
5VDIMM FOR DDR



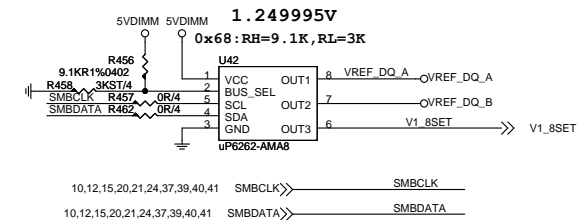
3VSB_WAKE



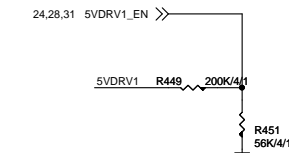
VCC1_5REF



UPI VOLTAGE CONSOLE (3)



USB MODE



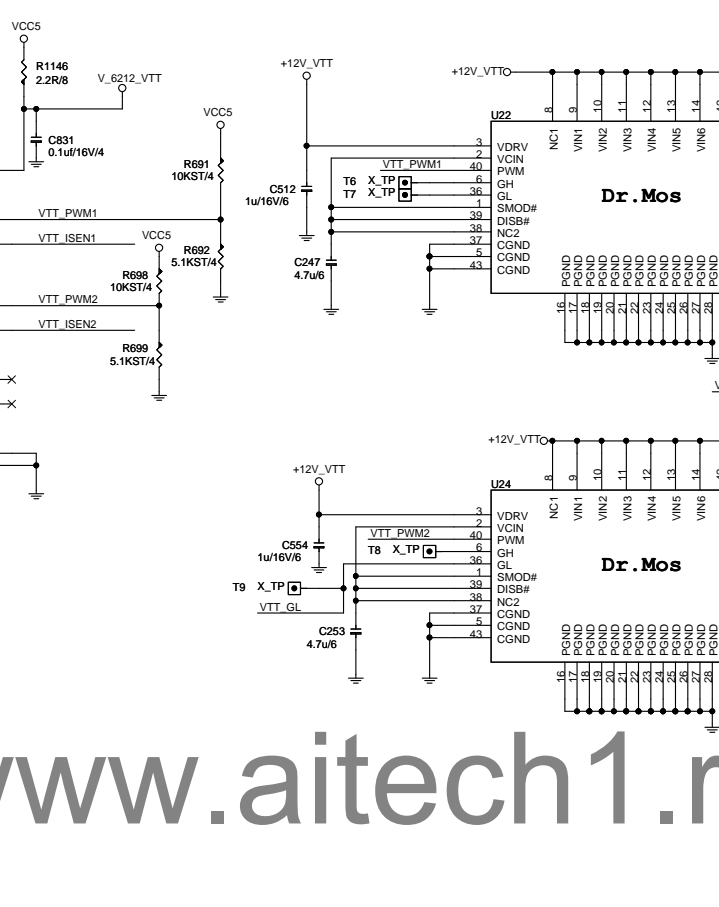
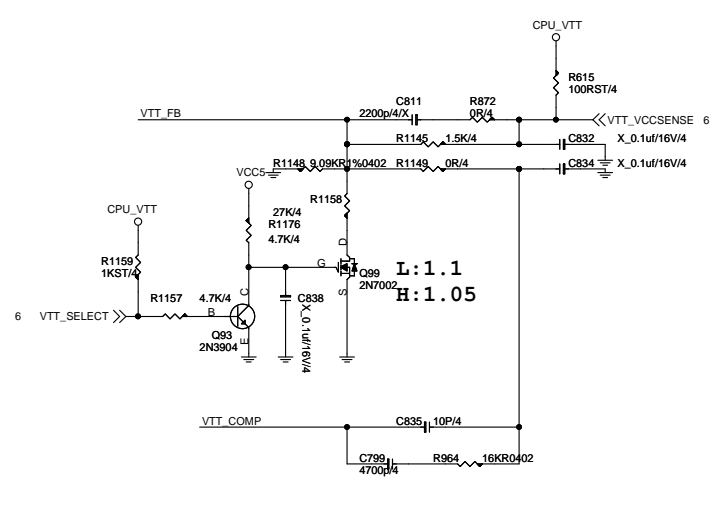
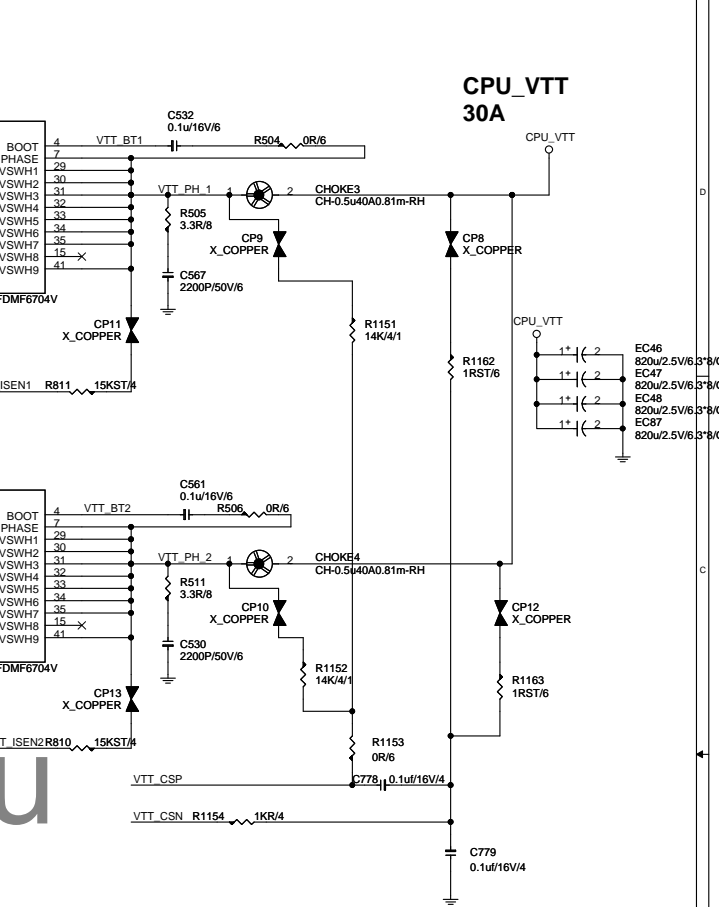
MICRO-STAR INT'L CO.,LTD		
MS-7585		
Size	Document Description	Rev
Custom	ACPI controller UPI	1.1

[illegible]

CPU_VTT STABLE TO VTTWRGOOD ASSERTION
MIN:100ns

Left Diagram: CPU_VTT is connected to R612 (1KRU/4). The other end of R612 is connected to VTT_PG D (6.37). A capacitor C244 (0.1uF/16V/4) is connected to the node between R612 and VTT_PG D.

Right Diagram: V_6212_VTT is connected to R522 (X_1MR/4). The other end of R522 is connected to VTT_IMON_R. A capacitor C574 (100P/16V/4) is connected to the node between R522 and VTT_IMON_R. A resistor R581 (24KST/4) is connected to the node between R522 and VTT_IMON_R.

[illegible][illegible]

DDR3_1.5V

10.75A

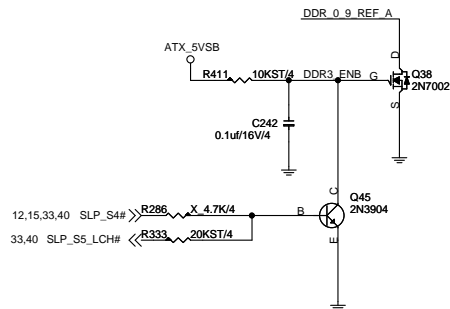
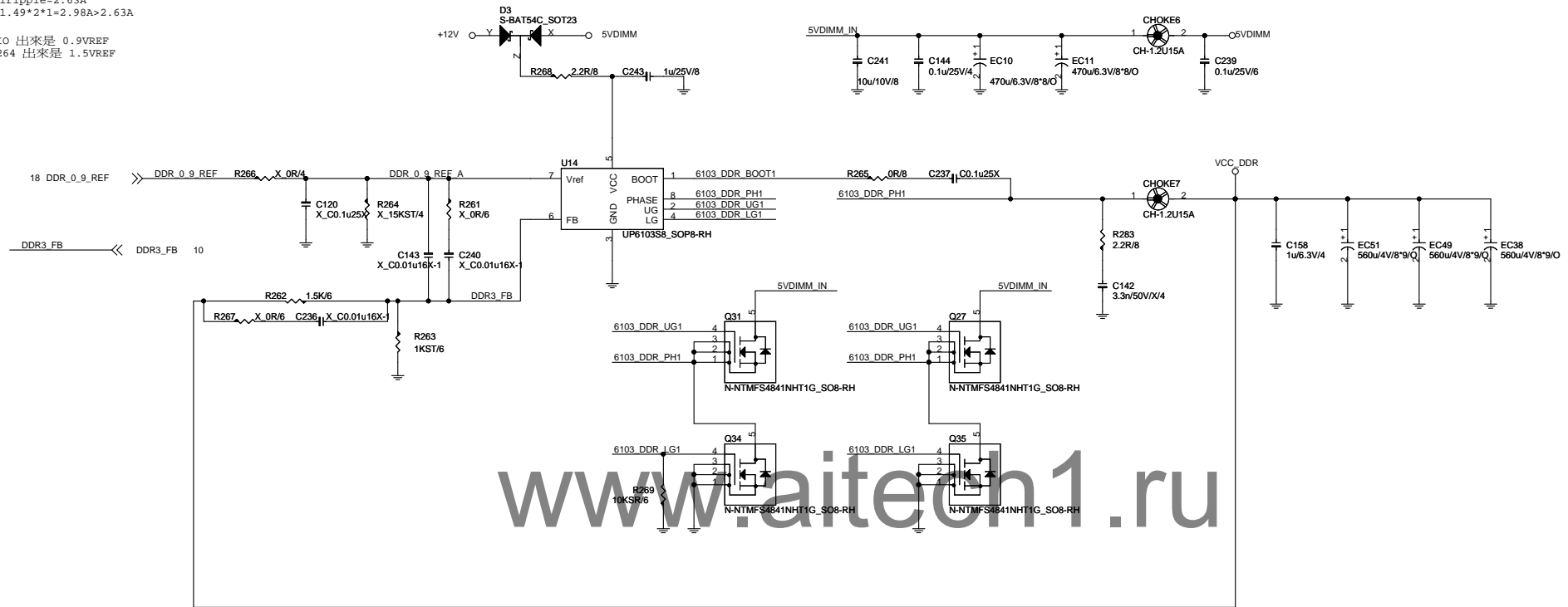
$$1.8A \times 4 + 2.5A + 0.75A = 10.75A$$

Iripple=2.63A

1.49*2*1=2.98A>2.63A

SIO 出來是 0.9VREF

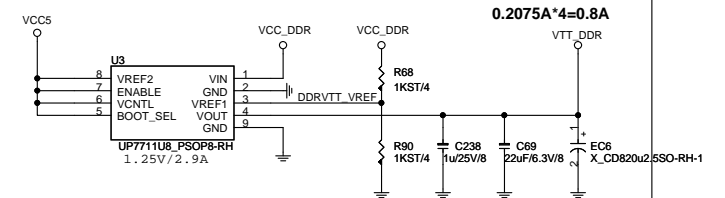
6264 出來是 1.5VREF



Only to meet Intel Power Down Sequence

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

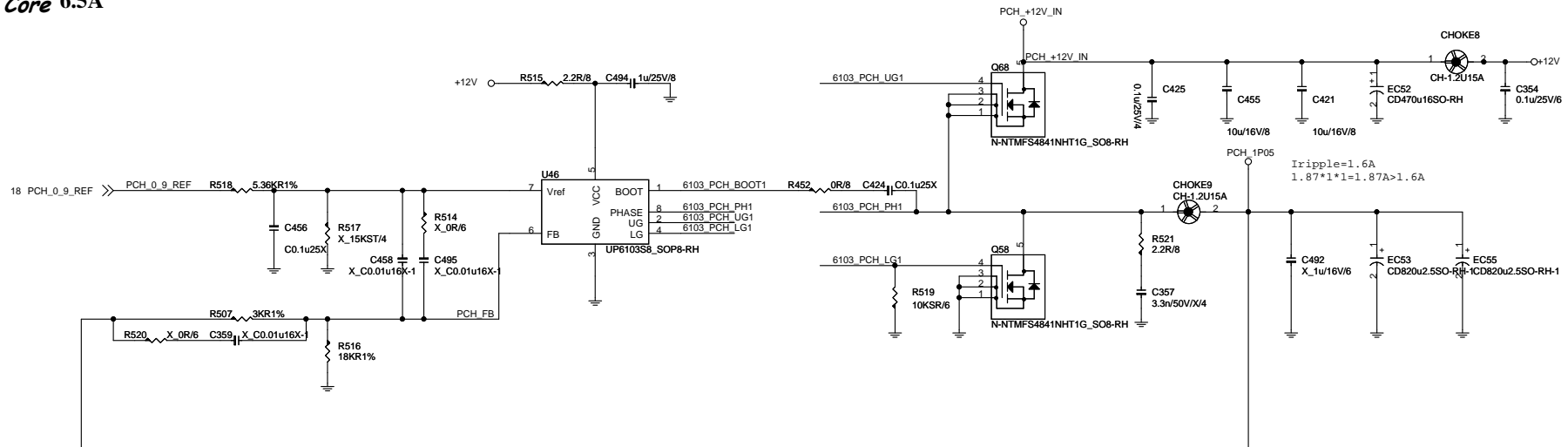


MICRO-STAR INT'L CO.,LTD

MS-7585

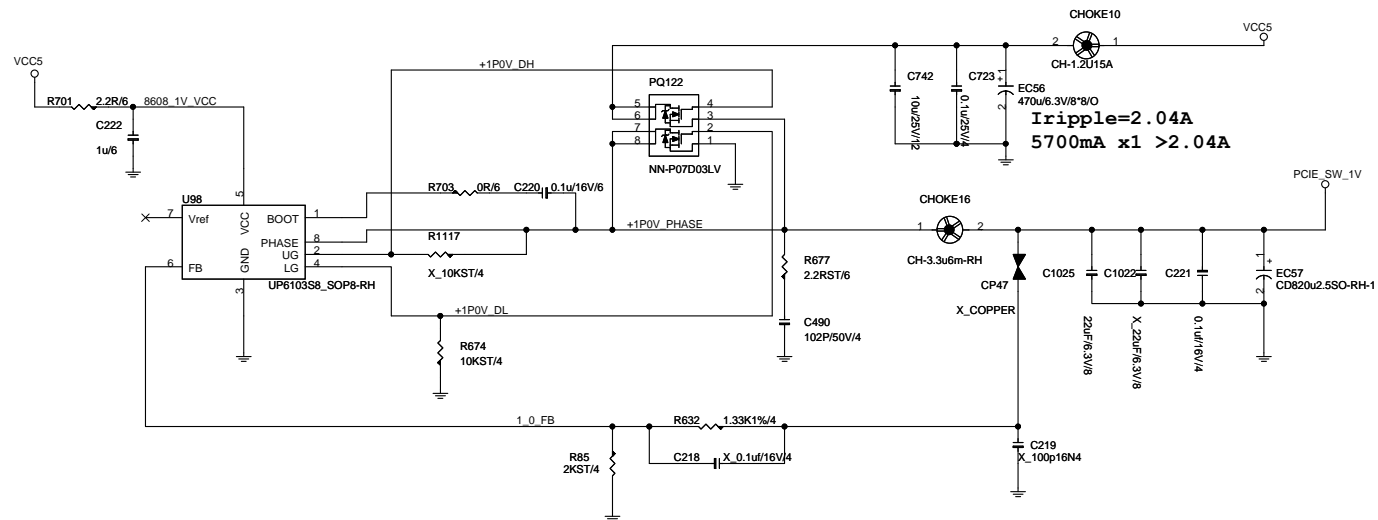
Size	Document Description	Rev
Custom	DDR Power - uP6103 1-Phase	1.1
Date: Wednesday, March 10, 2010	Sheet 35 of 48	

PCH Core 6.5A

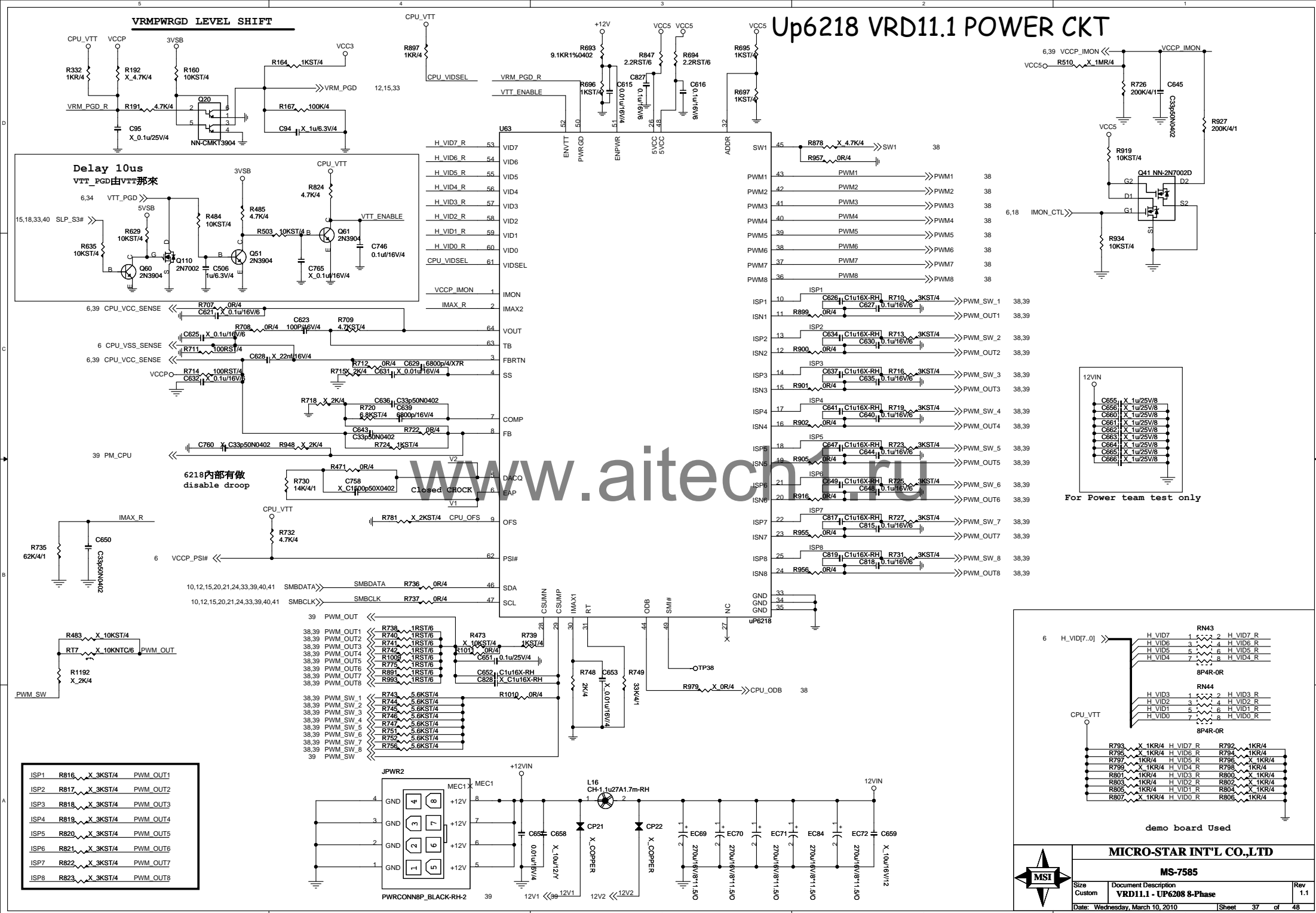


www.aitech1.ru

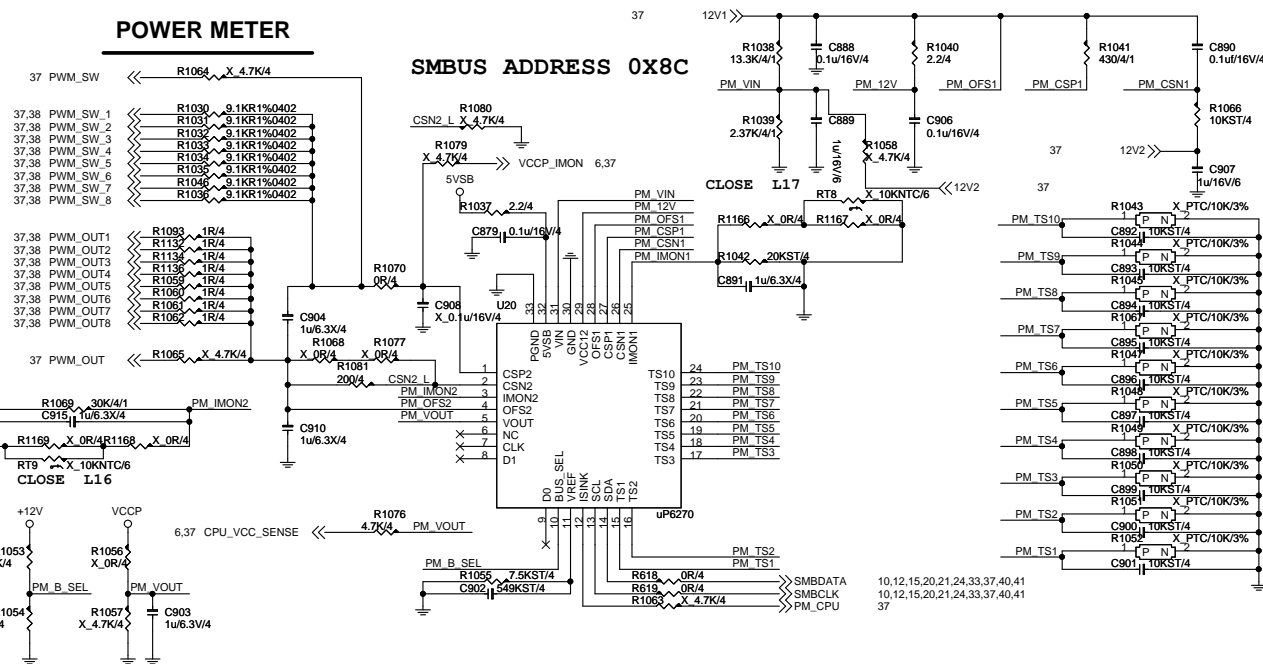
PCIE_SW_1V 3A



Up6218 VRD11.1 POWER CKT

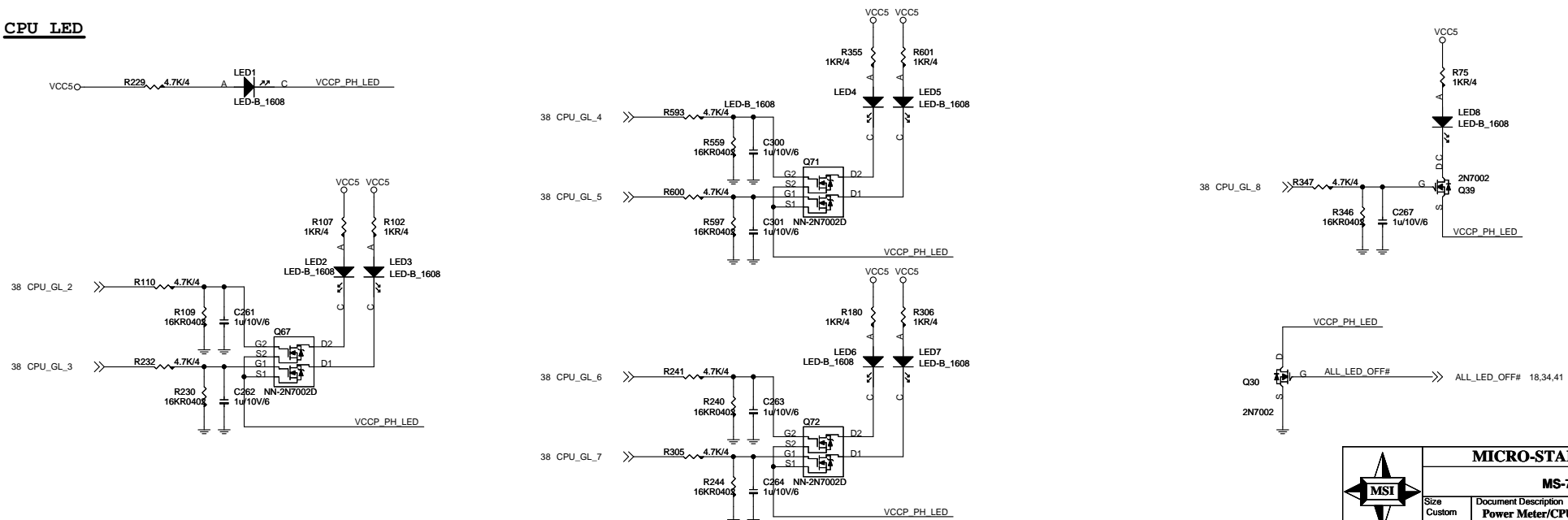


POWER METER



www.aitech1.ru

CPU LED



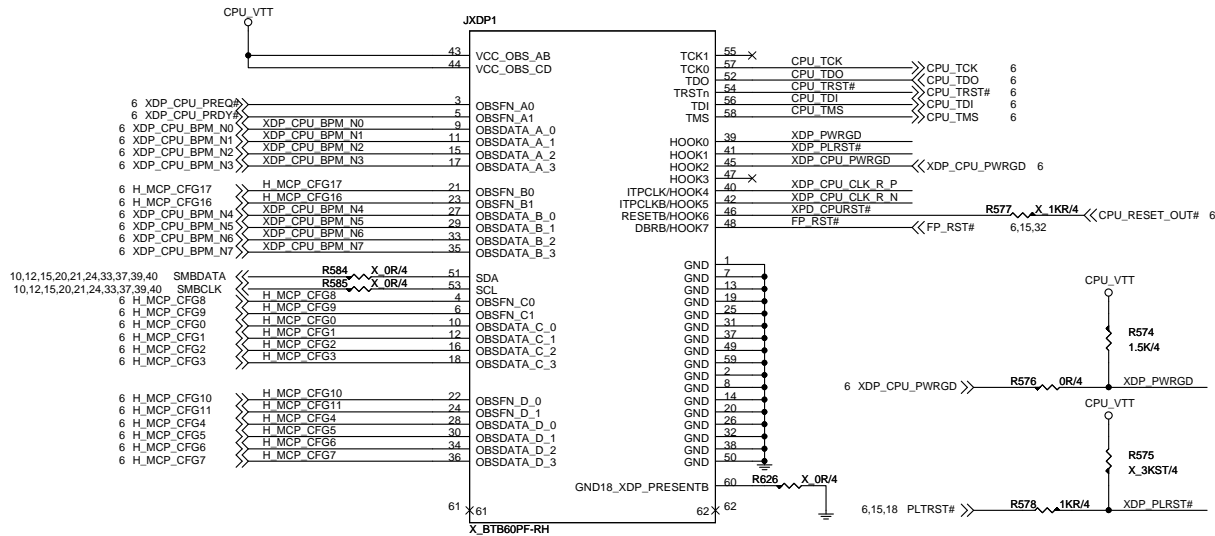
MICRO-STAR INT'L CO.,LTD

MS-7585

Size	Document Description
Custom	Power Meter/CPU LED CTL

Rev	
1.1	

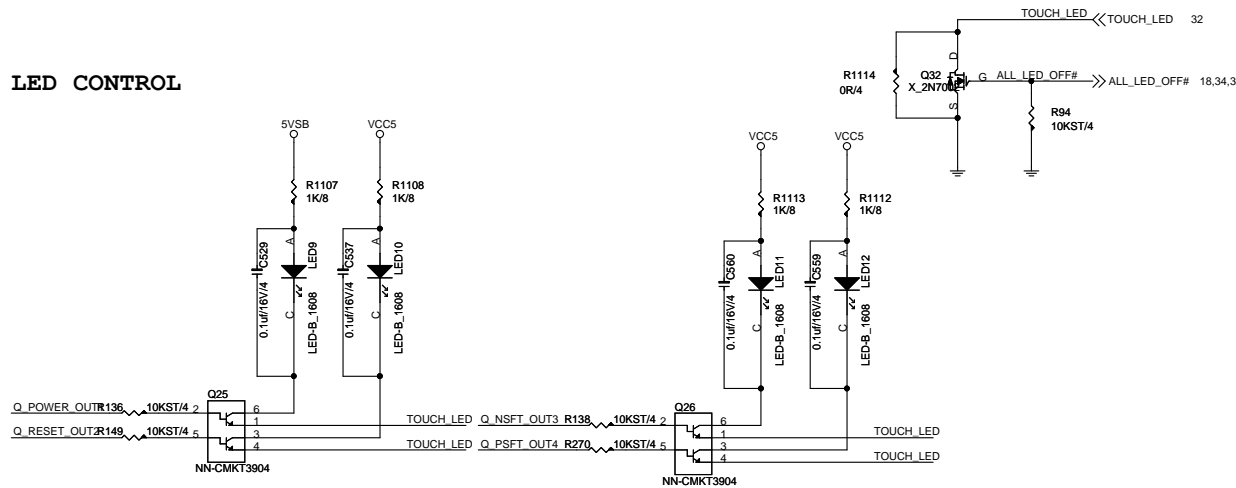
Reserve debug port 5020



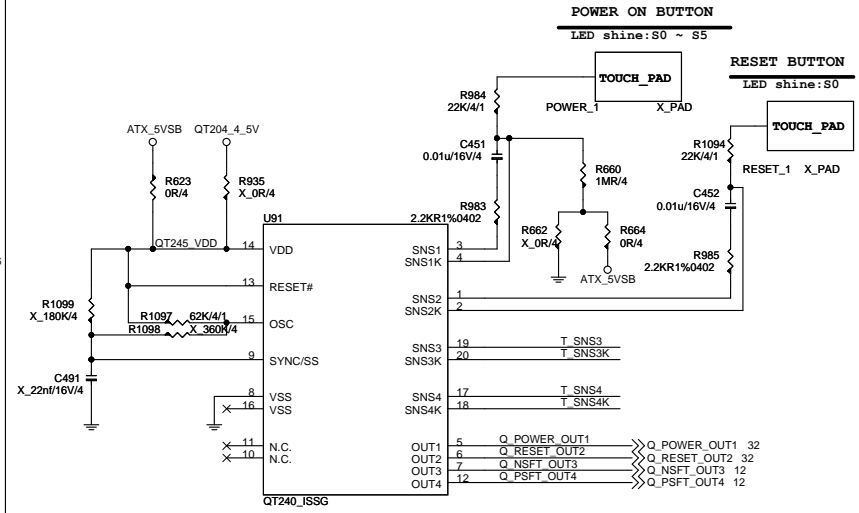
CPU XDP CLOCK



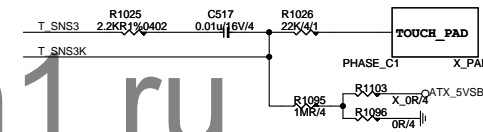
LED CONTROL



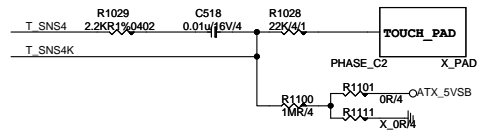
TOUCH PAD CIRCUIT



PHASE_C BUTTON



PHASE_D BUTTON

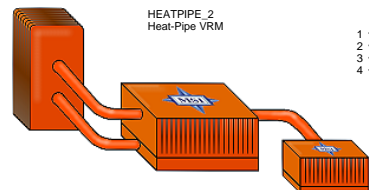
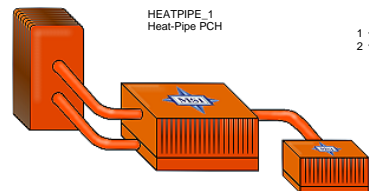


MICRO-STAR INT'L CO.,LTD

MS-7585

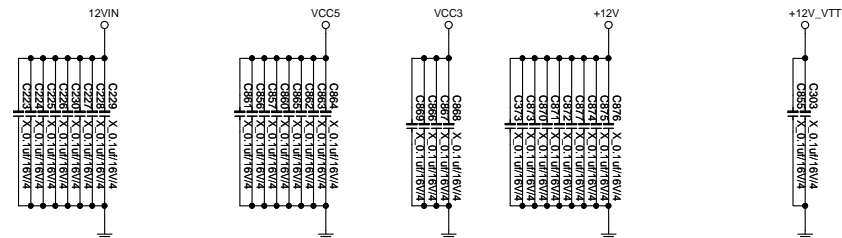
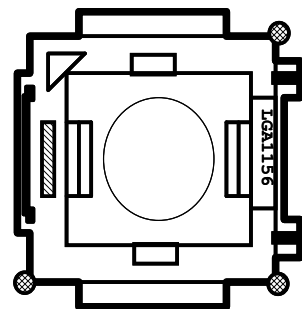
Size	Document Description	Rev
Custom	CPU/PCH XDP	1.1
Date: Wednesday, March 10, 2010	Sheet 41 of 48	

HEATPIPE

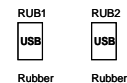
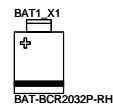


CPU SOCKET

CPU_H1
<HP-BOM>



BATTERY



外座



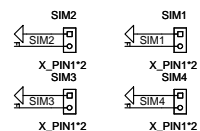
PCB



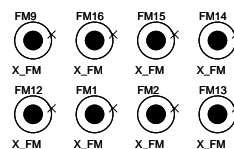
PD0-0758511-E55, 依頓, 23, 寶安恩斯邁廠 (MSIS)
PD0-0758511-G37, 精成, 23, 寶安恩斯邁廠 (MSIS)

www.aitech1.ru

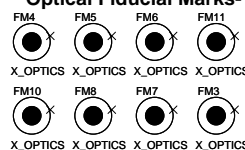
Simulation



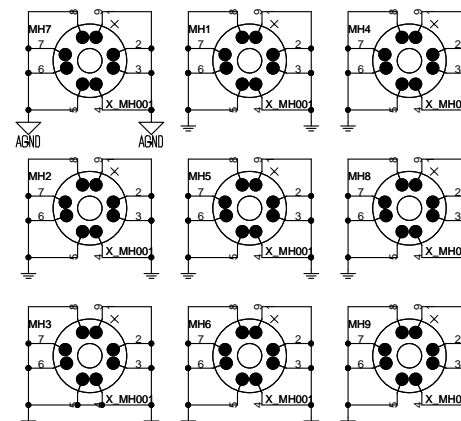
Optical Fiducial Marks-120



Optical Fiducial Marks-100



Mounting Holes



MICRO-STAR INT'L CO.,LTD		
MS-7585		
Size Custom	Document Description 8051_LED_control	Rev 1.1
Date: Wednesday, March 10, 2010 [Sheet 42 of 48]		